A hybrid Sigma-Delta modulator with reusable SAR quantizer

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Abstract: A novel energy-efficient hybrid multi-bit Sigma-Delta modulator with a reusable successive approximation register (SAR) quantizer is proposed. By reusing the SAR quantizer, sampling capacitors in the first integrator of the modulator could be eliminated and almost rail to rail input signal range could be achieved by the modulator without the requirement of a high-swing analog adder in front of the quantizer, which is usually power hungry in multi-bit modulators. In this way, small capacitors could be used to meet the thermal noise requirements, thus reducing the power and area consumption. With an improved switching procedure, only a half number of the unit capacitors are needed in the SAR quantizer, which further reduce the area consumption.

Keywords: Sigma-Delta modulator, successive approximation register, ADC, energy-efficient, CMOS

Classification: Integrated circuits

References


1 Introduction

The use of multi-bit quantization in Sigma-Delta modulators provides many advantages over their counterparts with single-bit quantization, such as reduced power dissipation, improved loop stability and enhanced performance. It has been becoming an attractive topology for Sigma-Delta analog-to-digital converters (ADCs) design in modern technology. In conventional multi-bit Sigma-Delta modulators [1], flash ADCs were usually used as the quantizers due to its minimum conversion latency. However, an exponential growth of power and area for each extra bit in flash quantizers makes them unsuitable for the low-power and high-compact circuits design. In addition, the offset mismatch among the constituent comparators in flash quantizers can degrade the resolution and linearity of the modulators. Several quantization techniques [2, 3, 4, 5] have been proposed to deal with those disadvantages in multi-bit Sigma-Delta modulators.

This paper presents a hybrid multi-bit Sigma-Delta modulator with a reusable SAR quantizer as shown in Fig. 1, in which the quantization, digital-to-analog conversion and summation in the dashed box could be realized by reusing only one SAR ADC. By using this new modulator structure with an asynchronous SAR quantizer using an improved switching scheme [6, 7, 8, 9, 10, 11, 12, 13], the number and value of capacitors can be reduced greatly. The requirements of the analog adder and dynamic element matching (DEM) circuits in the modulator can be relaxed, which introduces a significant reduction in the power consumption and area occupation.
2 Proposed hybrid modulator topology

To explain the proposed scheme, a second-order 5-bit hybrid sigma-delta modulator is used. It consists of a reusable 5-bit SAR quantizer and a two-stage integrator. Fig. 2 gives the circuit schematic and timing control. During the sampling phase of the modulator, the capacitor arrays of the SAR quantizer sample the input signal and meanwhile the capacitors CS sample the integrators output at the control of Clks. Following this sampling operation, SAR quantizer digitizes the sampled signal and the integrators output in a binary-search way under the control of SAR logic. The adder is accomplished through the charge summation by the capacitor Cs. After that, a residue $V_{RES}$ is generated on the top plate of the capacitor arrays.

$$V_{RES} = V_{IN} - V_{DOUT}$$  \hspace{1cm} (1)

where $V_{IN}$ is the sampled input signal and $V_{DOUT}$ is the quantized digital output. Then this residue is processed by the two-stage integrator during the integration phase of the modulator. And the digital output of the current sample $D_{OUT}(k)$ could be expressed as

$$D_{OUT}(k) = V_{IN}(k) + V_{RES}(k) \cdot H(k) + Q(k)$$  \hspace{1cm} (2)

where $H(k)$ is the transfer function of the integrator and $Q(k)$ represents both the quantization noise and the comparator noise of the quantizer. Substituting (1) into (2) and performing a z-transform, we obtain the following system transfer function (3), which is the same transfer function as the conventional modulator shown in Fig. 1. An all-pass signal transfer function (STF) and a high-pass noise transfer function (NTF), which shape both the quantization noise and comparator noise could be got from the proposed modulator.

The reusable SAR quantizer in the proposed modulator is based on an asynchronous SAR ADC. A high frequency off-chip clock is avoided by using an asynchronous clock generator just like the one in [6]. The working procedure could be divided into three phases: sampling, redistribution and analog-to-digital conversion. An improved switching scheme is proposed in the SAR quantizer to reduce the switching energy and the number of unit capacitors. The number of unit capacitors could be reduced by a half compared to the converters that use the conventional switching procedure. It means only 16 unit capacitors are needed to fulfill a 5-bit analog-to-digital conversion, which simplifies the dynamic element matching circuit by a half. Waveform of the improved switching procedure is shown in Fig. 3. The final 5th-bit residue error is captured by switching only one.
side of the last unit capacitor as shown in the dashed circle of the figure, rather than keeping it unchanged during the conversion phase like the conventional one.

3 Simulation results

The example modulator is designed in a 0.18 µm CMOS technology. It consumes only 132 µW with a 1.8 V supply voltage. The effective OSR is 64. Fig. 4 and Fig. 5 show the simulation output spectrum and SNDR versus input signal level characteristics of the modulator. A 112 dB SFDR and 103 dB SNDR were achieved with a 5.078125 kHz 3.5 Vpp sinusoidal input signal. As depicted in the figure, overload level of the modulator closes 1. In other words, with a rail-to-rail reference voltage, a rail-to-rail input signal range could be provided by the modulator. Fig. 6
presents the output level of the integrator stages and quantizer with the amplitude of the input sinusoidal signal set near to full range of the reference level. The peak to peak output level of the two integrator stages is smaller than 200 mV, which helps to relax the performance requirements of op amps in integrator, significantly.

Fig. 4. Simulation output spectrum with a sinusoidal input

Fig. 5. Simulation SNDR versus input level plots

Fig. 6. Simulation output level of different integrator stages and the quantizer
4 Conclusions

A novel hybrid multi-bit SAR-Sigma-Delta modulator with reusable SAR quantizer is proposed. The reusable SAR quantizer and an improved switching procedure result in a low-power and area-efficient high-performance Sigma-Delta modulator. The circuit simulations verify the effectiveness of the proposed modulator.

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