Inverter-based sigma-delta modulator based on three-phase clock technique

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Abstract: A low-voltage inverter-based sigma-delta modulator (SDM) based on a three-phase clock technique is presented. The three-phase clock is proposed to mitigate a performance degradation due to a gate leakage current in advanced process nodes, which reduces noise introduced by the charge injection at the end of a sampling phase and an integrating phase. Simulation results in a 65 nm CMOS process show that the spectrum characteristics of the SDM match well the MATLAB model and achieve 5.1-dB enhancement in the signal-to-noise and distortion ratio performance compared to a traditional inverter-based SDM implementing the uniform loop filter and the same oversampling ratio.

Keywords: sigma-delta modulation, switched-capacitor circuit, class-C inverter, gate leakage current, deep-submicrometer process

Classification: Integrated circuits

References

1 Introduction

With a scaling feature size and a supply voltage reduction in CMOS processes, a design of an operational transconductance amplifier (OTA) has become a main bottleneck in switched-capacitor (SC) sigma-delta modulators (SDMs). An attractive method for designing a low-voltage SDM is inverters utilized instead of conventional OTAs [1, 2, 3]. However, a gate leakage current cannot be neglected for CMOS processes below 90 nm [4], which leads to a charge error for inverter-based SC circuits such that the performance degrades. High voltage I/O devices can be adopted to deal with this issue at the cost of power consumption [5].

In this work, a three-phase clock technique is proposed to reduce the charge error due to the gate leakage current. Compared with the traditional inverter-based SC integrator [2], this technique reduces the voltage variation on the auto-zeroing capacitor by 2.16 mV and minimizes the noise. Two second-order inverter-based SC SDMs implementing the uniform loop filter and the same oversampling ratio (OSR) with a conventional two-phase non-overlapping clock and the three-phase clock technique are designed in a 65 nm CMOS process. This technique has a signal-to-noise and distortion ratio (SNDR) improvement of 5.1 dB compared with the conventional counterpart. Moreover, the noise floor of the output spectrum based on the three-phase clock matches well the MATLAB model.

2 Operation principle of inverter-based SC integrator with three-phase clock

2.1 Conventional inverter-based SC integrator

The conventional inverter-based SC integrator using two inverter amplifiers with two non-overlapped clock phases, the sampling phase $\phi_1$ and the integrating phase $\phi_2$, along with delayed counterparts $\phi_{1D}$ and $\phi_{2D}$, is shown in Fig. 1(a). During $\phi_1$, the integrator input $V_{IN}$ is sampled in the sampling capacitor $C_S$, and the offset voltage $V_{OFF}$ is sampled in the auto-zeroing capacitor $C_C$. During $\phi_2$, the inverter input $V_X$ should hold $V_{OFF}$ owing to a negative feedback formed through the integrating capacitor $C_I$, which forces $V_G$ to be a virtual ground. Thus, the charge is transferred from $C_S$ to $C_I$ [2]. To avoid output common-mode (CM) voltage drift from the power supply variation and the charge injection, a passive CM feedback circuit is realized through the capacitor $C_M$ [6]. Fig. 1(b) indicates the operation of the conventional inverter-based SC integrator at the end of $\phi_{1D}$. Since a path exists for electrons to flow into or out of the node X due to the gate leakage current, the sampling switch $S_1$ injects a charge packet $Q_1$ onto $C_S$ and $C_C$, which makes the integrator lossy and considerably deteriorates the in-band quantization noise.
Moreover, this charge error is unknown and sensitive to the device geometry size, the signal frequency and the supply voltage, which introduces extra noise. As a result, the noise floor of the output spectrum will be raised.

2.2 Inverter-based SDM with the three-phase clock

Fig. 2 shows the inverter-based SC integrator with the three-phase clock and its timing diagram. Charge transfer manner is consistent with the conventional one described above. The clock scheme includes a third phase \( \theta_3 \) that can reduce the influence of the gate leakage current in deep-submicrometer CMOS processes. When sampling switches and integrating switches turn off, there is a negative pulse on \( \theta_3 \) such that no resistive path exists at the node X. Hence, the integrator lossy and the extra noise caused by the gate leakage current are mitigated. \( \theta_3 \) occurs between \( \theta_1 \) and \( \theta_2 \) which does not increase conversion time.

3 Circuit implementation details

This section describes the implementations of the SDM which employ the inverter-based SC integrators with the three-phase clock. Fig. 3(a) shows the z-domain
model of the classical single-bit second-order modulator with a cascade of integrators with a feedforward (CIFF) [7] architecture. Fig. 3(b) shows the schematic of the SDM using a pseudo-differential topology with the three-phase clock. The supply voltage is selected to be a little lower than the summation of the threshold voltage of the inverter input transistors such that the inverter behaves as a micro-power class-C amplifier. At the beginning of $\theta_2$, one of the input transistors in the inverter operates in the strong inversion region while the other is completely off depending on the polarity of input single. At other time, all transistors operate in the weak inversion region. The type of the capacitor is metal-oxide-metal (MOM) capacitor. A simplified circuit is used to generate the three-phase clock, which uses only logic circuits and does not need a complicated state machine.

![Fig. 3. (a) SDM architecture, (b) SDM schematic](image)

When the SDM is designed in a 65 nm process, the leakage current of the switch implemented by the 1.2 V low threshold voltage ($V_{th}$) MOS device may cause a loss of the integrator operated at a low sampling frequency for sensor applications, and therefor degrades the performance [8, 9]. If 1.2 V high $V_{th}$ MOS devices or 1.8 V I/O devices are used to implement the switch, the signal distortion should appear in SDM operated at a low supply voltage. According to simulation results, the leakage current of 1.2 V standard $V_{th}$ NMOS and PMOS are 30 pA/µm and 0.265 pA/µm, respectively, under a supply voltage of 0.8 V. At an operating frequency of 35 kHz, those switches implemented by 1.2 V standard $V_{th}$ MOS device achieve low enough leakage current and switch closed resistance.

### 3.1 Gain-boost class-C inverter

For some high-resolution applications, the simple inverter and the conventional cascade inverter can not provide enough high direct current (DC) gain [10]. Fig. 4(a) shows a gain-boost inverter. Transistors M1, M3, M5 and M7 (M2, M4, M6 and M8) form a current-current feedback loop, which increases the output impedance and the DC gain. As mentioned above, its nominal supply voltage is
0.8 V. To operate as a class-C inverter (the supply voltage is less than or equal to the sum of the absolute threshold voltage of the input transistors), M1 and M2 employ 1.2 V standard $V_{th}$ MOS devices. At a typical corner, the threshold voltage of M1 and M2 are 0.425 V and $-0.409$ V, respectively. To optimize the output swing, M3 and M4 use 1.2 V low $V_{th}$ MOS devices. At a typical corner, the threshold voltage of M3 and M4 are 0.25 V and $-0.27$ V, respectively. Simulation results show a DC gain of 85 dB, a unity gain bandwidth of 400 kHz and a phase margin of 85° with a load capacitor of 2 pF. When the inverter output varies from 0.16 to 0.61 V, the gain-boost inverter keeps a larger DC gain than 60 dB.

3.2 Comparator

Since the nonidealities of the single-bit quantizer experience a noise shaping by the SDM, the performance requirements on the quantizer are not stringent. A regenerative latch comparator is adopted to realize the quantizer, as shown in Fig. 4(b), which consists of a regenerating latch and a SR latch. When the comparator is not active ($\theta_{1DD} = 0$), the regenerating latch is reset and has almost no power consumption; the output voltages (OUT$_P$ and OUT$_N$) are latched by the SR latch. When the $\theta_1$ is asserted ($\theta_{1DD} = 1$), the input voltages (IN$_N$ and IN$_P$) cause one of the comparator outputs to be high and the other to be low. Simulation results show a propagation delay time of 200 ps and an accuracy of 60 nV.

4 Simulation results

The proposed three-phase clock-controlled inverter-based SC SDM is designed in a 65 nm CMOS process, along with a conventional inverter-based SC SDM implementing the uniform loop filter and the same OSR. Fig. 5(a) shows the time-domain waveform of phase $\theta_{1D}$ and differential voltage on the auto-zeroing capacitor $C_{C1}$ with the conventional two-phase non-overlapping clock and the proposed three-phase clock. The SDM with the three-phase clock has a differential voltage variation on the capacitor $C_{C1}$ of 0.34 mV compared to 2.5 mV in the conventional one. Fig. 5(b) shows the output spectrums of three SDMs using the conventional two-phase non-overlapping clock, the three-phase clock and the MATLAB model. Comparing with the conventional design, the noise floor of the
output spectrum of the three-phase clock-controlled SDM is significantly reduced. The SNDR shows 5.1-dB improvement in performance. Furthermore, the spectrum characteristics of the proposed SDM match well the MATLAB model.

![Fig. 5](image)

Fig. 5. (a) Time-domain waveform of phase θD and differential voltage on capacitor C1, (b) Output spectrums of three SDMs for −6-dBFS, 51-Hz sine-wave input with 130-Hz bandwith and 35-kHz sampling frequency

5 Conclusion

We present a low-voltage SC inverter-based SDM using a three-phase clock. The three-phase clock technique reduces the influence of the gate leakage current in deep-submicrometer CMOS processes. A SNDR improvement of 5.1 dB can be achieved compared to a conventional inverter-based SDM implementing the uniform loop filter and the same OSR. The noise floor of the output spectrum of the proposed SDM matches well the MATLAB model and is less than that of the conventional scheme. Moreover, this technique does not increase the complexity of the circuit and conversion time. It has an attractive potential to be used to design SDM using deep-submicrometer CMOS processes.

Acknowledgments

This work has been supported by the National Natural Science Foundation of China (No. 61471119), Priority Academic Program Development of Jiangsu Higher Education Institutions, Topnotch Academic Programs Project of Jiangsu Higher Education Institutions (PPZY2015A035) and Academic Degree Postgraduate Innovation Project of Jiangsu Regular University (KYLX16-0215).