A triple-bias parallel SSHI rectifier for piezoelectric energy harvesting

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Abstract The traditional SSHI circuit forms a resonant loop to salvage the charges that would otherwise be wasted. However, the quality factor of the loop would be low. This brief presents a triple-bias parallel SSHI rectifier, which can effectively enhance the power extraction capability from the piezoelectric (PE) transducer. The circuit has a low complexity and is easy to integrate, which can convert the original one voltage flipping into a triple per half cycle, thereby improving the voltage flipping ratio for low quality factor. The experimental results show that, compared to the traditional SSHI circuit, the power obtained by the load is boosted up to 1.23 X.

Keywords: piezoelectric energy harvesting, SSHI, multi-bias, rectifier

Classification: Energy harvesting devices, circuits and modules

1. Introduction

Due to the advantages of high power density, versatile shape and good compatibility with miniaturization, piezoelectric (PE) transducer has been widely used in vibration energy harvesting [1] for applications such as wireless sensor nodes (WSNs) [2]. Advanced technology has strongly promoted the development of on-chip self-powered microsystems such as Piezoelectric Micro-Electro-Mechanical Systems (PiezoMEMS) for the next generation [3, 4]. However, the internal capacitor of the PE transducer poses a unique challenge to the design of the PE energy harvesting circuit.

Let’s assume the dotted capacitor $C_b$ is shorted now. Fig. 1 shows a typical parallel SSHI rectifier, consisting of a synchronized switch harvesting on inductor (SSHI) circuit, and full-bridge rectifier. The SSHI circuit can significantly enhance the power extraction from the small-scale PE transducer [5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16]. The reason is that the SSHI circuit forms the resonant loop (L-$C_p$-SW-L) can salvage the charges in the capacitor $C_p$ that would otherwise be wasted. To further reduce the loss, [17, 18, 19, 20, 21] adopt the active diodes for the rectification instead of passive ones. However, the efficiency of the SSHI circuit is sensitive to the quality factor $Q$ of the loop, which results in the voltage can not be completely flipped [14]. Recently, some researchers paid attention to this issue and reported several improved schemes.

![Fig. 1. A typical parallel SSHI rectifier](image)

The scheme that converts the original one voltage flipping into a multiple per half cycle has attracted the interest. Liang et al. in [22] proposed the conceptual circuit, and then the circuit was visualized in [23, 24]. The circuit was implemented using discrete components, so it is not easy to be simplified and integrated. Du et al. in [25, 26] used the switched-capacitor circuit across the PE transducer to achieve multiple voltage flipping. Due to without using the inductor in the loop, the energy losses are relatively large. Chen et al. in [27] fully integrated the rectifier with multiple voltage flipping. The common in [23, 24, 25, 26, 27] is essential to the insertion of the appropriate dashed capacitor $C_b$ with initial voltage as shown in Fig. 1 into the loop, to convert single voltage flipping into a multiple.

This brief presents a triple-bias parallel SSHI rectifier, which adopts switched-capacitors and active diodes. The circuit can realize voltage flipping with the triple-bias. As the rectification and voltage flipping do not overlap in time, it is feasible to share the switches that originally used for the rectification (i.e., transferring energy into the load) for the SSHI operation. Furthermore, only one switch in series with one capacitor across one upper arm of full-bridge topology, without any other components, the circuit is simple and hence low complexity.

2. Preliminaries

We modeled the PE transducer using lumped parameters [28] and further simplify the model as shown in Fig. 1 due to low $C_p$ [29]. Consider the diodes in full-bridge rectifier are ideal and the load filter capacitor is relative large with
having the stable voltage of $v_{rect}$. Fig. 2(a) shows the key waveforms of SSHI schemes with a single-bias of 0 V (typical SSHI) and the triple-bias for voltage flipping during steady state operation, including voltage $v_{BA}$ and current $i_L$ (see Fig. 1). To distinguish between the schemes, the close-up views of the waveforms of the inductor current $i_L$ and voltage $v_{BA}$ are shown in Fig. 2(a). As can be seen in Fig. 2(a), an important point is that the voltage $v_{BA}$ drops from $V_{rect}$ to $-V_f$ rather than to $-V_{rect}$, which implies the voltage can not be completely flipped for both schemes. However, unlike the single-bias scheme, the triple-bias scheme converts the original one voltage flipping into a triple per half cycle. In steady state, the features of the triple-bias scheme can be summarized as follows: 1) once the small voltage flipping is performed each time, the current $i_L$ just happens to have a half wave, 2) the value of the capacitor voltage $v_b$ is not constant, and is the function of the peak inductor current of $i_L$, 3) the number of voltage bias $v_b$ is the same as that of voltage flips, and 4) the voltage $v_{BA}$ is flipped sequentially one by one till the last one. Therefore, the SSHI scheme with the single-bias is a special case of with the triple-bias.

Fig. 2(b) is an equivalent resonant circuit formed and used by the SSHI circuit with the triple-bias. The capacitor $C_P$, the inductor $L$ and the switch SW shown in Fig. 2(b) are also shown in Fig. 1. Here, $R$ is the total parasitic resistance along the resonant loop, and $C_b$ is the inserted capacitor with an initial voltage. The value of the $C_b$ is relatively large such that the voltage $v_b$ does not change much during the voltage flipping, and hence it behaves like a voltage source. Assume that the switch SW is OFF and $v_{rect}(0^-) = V_{rect}$, $v_b(0^-) = 0$ initially, where $V_{rect}$ is rectifier output voltage and $v_b$ is the set bias-voltage. When the switch SW is ON, the voltage $v_{BA}$ can be expressed as

$$v_{BA}(t) = (V_{rect} - V_b) \frac{\theta_0}{\theta_d} e^{-at} \cos(\omega_d t + \theta) + V_b$$  \hspace{1cm} (1)$$

Where $a = \frac{2R}{LC}$, $\theta_0 = \frac{1}{\sqrt{\omega_d}}$, $\omega_d = \sqrt{\omega_0^2 - \alpha^2}$ and $\theta = \arccos\left(\frac{\omega_0}{\omega_d}\right)$.

From Equ. (1), we know that the voltage $V_b$ sets the bias voltage for oscillation and also determines a voltage flipping magnitude. Referring to Fig. 2(a), we can define the voltage flipping ratio $q_F$ as

$$q_F = \frac{|V_f|}{|V_{rect}|}$$  \hspace{1cm} (2)$$

Here, note that $V_f$ is the final flipped voltage regardless of how many times the voltage is flipped in each half cycle, i.e., the voltage difference $\Delta V$ between ideal and actual for the flipped voltage is $V_{rect} - |V_f|$ after completing the whole process of voltage flipping. The range of the value $q_F$ is $0 < q_F < 1$. The energy losses during the process can be expressed as

$$E_{loss} = \frac{1}{2} C_P V_{rect}^2 - \frac{1}{2} C_P(q_F V_{rect})^2 = \frac{1}{2} C_P V_{rect}^2 (1 - q_F^2)$$  \hspace{1cm} (3)$$

From Equ. (3), we know the larger $q_F$, and lower energy losses $E_{loss}$ per half cycle.

For the $E_{loss}$, the comparative analysis between the SSHI schemes with the single-bias and the triple-bias is as follows. For both cases, assume that the resonant circuit in use has the same quality factor $Q$. As shown in Fig. 2(a), suppose that the voltage $v_{BA}$ is flipped from initial voltage $V_{rect}$ for both schemes. For relatively large Q, the voltage flipping ratio $q_{F,SB}$ for the SSHI with the single-bias is readily obtained as \cite{14}

$$q_{F,SB} = e^{-\frac{\alpha}{\sqrt{Q}}}$$  \hspace{1cm} (4)$$

As $Q = \frac{1}{h} \sqrt{\frac{L}{C_P}}$, $q_{F,SB}$ is only related to the characteristic of the resonant loop, i.e., $Q$.

According to the Ericsson cycles, if each voltage flipping keeps the same, then the efficiency is the best. So, under the assumption of the same Q used for the loop, the voltage flipping ratio $q_{F,MB}$ for the triple-bias SSHI, i.e.,
the ratio of voltage span for the voltage $v_{BA}$ before crossing the zero point to after crossing the zero point, is readily obtained as

$$q_{F,MB} = \frac{1 + 2q_{F,SB}}{2 + q_{F,SB}}$$

(5)

Due to $0 < q_{F,SB} < 1$, we can get $q_{F,MB} > q_{F,SB}$. Therefore, compared to the single-bias, the SSHI with the triple-bias improve the voltage flipping $q_F$ and hence lower energy losses $E_{loss}$ per half cycle.

3. Proposed triple-bias parallel SSHI rectifier

Fig. 3(a) shows the design of the triple-bias parallel SSHI rectifier, which consists of an inductor (L), four switches ($S_1$-$S_4$), two capacitors ($C_1$-$C_2$) and two active diodes ($D_1$-$D_2$). The active diode is composed of a comparator and an NMOS as shown in the dashed box in Fig. 3(a). Compared to the passive diode, the advantage of using the active diode is less voltage drop and hence smaller conduction losses when the current flows through it. However, the active diodes have some non-ideal factors and consume the power. Hence, from a practical point of view, it is prudent to design the active diode and not lose too much in terms of efficiency. More detail for non-ideal cases refers to [30]. Note that the capacitors $C_L$, $C_1$ and $C_2$ are large to remain relatively stable voltages.

For the sake of illustration, suppose that the signal (i.e. the signal $S_1$ in Fig. 3(b)) is high to turn on the corresponding switch (i.e. the switch $S_1$ in Fig. 3(a)), and vice versa. The operation refers to the waveforms in Fig. 3(b). Before $t_{0}$, the switch $S_2$ is ON, the active diode $D_1$ is turned on, other switches $S_1$, $S_3$, and $S_4$ are OFF, and the current $i_p$ flows into the load $R_L$ via $D_1$-$Transducer$-$S_2$. Now, when $i_p$ asymptotically closes to the zero point, the $D_1$ is turned off. This leads that the $S_3$ is ON, the node voltage at A is pulled up to $v_{rect} - v_{c1}$, and the first resonant loop ($S_2$-$C_1$-$Transducer$-$S_2$-$L$-$S_3$) is formed. The partial energy stored in $C_P$ is transferred to the inductor L, and then the inductor energy is transferred back to $C_P$, which results in a sharp drop voltage of $v_{BA}$. Owing to the capacitor $C_1$ in the loop, the voltage $v_{BA}$ is flipped based on the bias-voltage of $v_{c1}$. Once the loop current $i_L$ returns to 0, i.e. $v_{BA}$ drops to a local minimum, the $S_3$ is OFF and the $S_1$ is ON, and the second resonant loop ($S_1$-$Transducer$-$C_2$-$S_2$) is formed, further dropping the voltage of $v_{BA}$. Similarly, as the current $i_L$ returns to zero again, the $S_2$ is OFF and the $S_4$ is ON, the last resonant loop ($S_2$-$C_1$-$S_1$-$Transducer$-$C_2$-$S_4$) is formed, and the voltage $v_{BA}$ finally drops to the minimum value. Until now, the voltage flipping process per half cycle is completed. Then, after $t_3$, the capacitor $C_P$ is charged negatively by negative current $i_p$, such that the node voltage at B decreases. Once it falls below zero voltage, the $D_2$ is turned on, and $i_P$ flows to the load $R_L$ via $D_2$-$Transducer$-$S_1$. The similar process occurs in the next negative half cycle but using different other two resonant loops due to the symmetrical operations. It should be noted that the capacitor $C_1$($C_2$) is charged (discharged) during the positive half cycle of $i_p$ and discharged (charged) during the negative half cycle, and so the voltages of $v_{c1}$ and $v_{c2}$ eventually attain a stable value. In addition, the switches $S_1$-$S_4$ are sized the same, and so a constant-on time module can be used for the switch timing, which results in a simple controller. In our design, only two OR gates, two RS flip-flops and six constant-on time modules were used.

4. Experiment results

We designed the proposed circuit using 0.35 µm CMOS process. The simple model of the PE transducer as shown in Fig 1 was used for simulation, in which $i_p = 100 \mu A \cdot \sin(2\pi f_p)$, $f_p = 100$ Hz, $C_P = 19$ nF, $R_P = 600$ kΩ. The load $R_L = 70$ kΩ and $C_L = 500$ nF. The capacitor $C_{1(2)} = 500$-nF.
Fig. 4 shows the key waveforms of the triple-bias SSHI rectifier and their zoom-in views. The amplitude of the current \(i_p\) is 100 \(\mu\)A initially, and it is changed to 70 \(\mu\)A after 2 s for the transient. Due to the capacitor voltages \(v_{c1}\) and \(v_{c2}\) are zero at \(t = 0\), the voltages gradually rise during the period of \(0\)–\(1\) s, and finally attain the stable voltage of 2.65 V around 1 s, i.e., at this point, absorbed (released) energy in \(C_1(C_2)\) during the positive cycle is equal to released (absorbed) energy during the negative cycle. The zoom-in views of the waveforms during steady state operation are given in the box on the right side of the Fig. 4. During the zero-crossing point of the current \(i_p\), the voltage \(v_{c1}\) is slightly increased as being charged, and the waveforms of the voltage \(v_b\) and the current \(i_L\) as expected.

Fig. 5 shows obtained power by the SSHI schemes for cases with the single-bias and with the triple-bias under the same excitation condition. As the load voltage \(V_{rect}\) increases, the power obtained by the load also increases, and the voltage is, however, limited by the breakdown voltage of the process. The maximum obtained power for the two schemes occurs at \(V_{rect}\) of 5 V, and their values are 257.1 \(\mu\)W and 208.8 \(\mu\)W respectively. It indicates the power obtained for the triple-bias SSHI rectifier is boosted up to 1.23 X, compared to the traditional single-bias SSHI rectifier.

5. Conclusion

A triple-bias SSHI rectifier for piezoelectric energy harvesting is presented. The proposed circuit is designed using a 0.35 \(\mu\)m CMOS process. The key advantage of the proposed design is simple and easy to integrate. The experimental results show that the performance of the circuit is better than that of the traditional SSHI circuit under the same excitation condition, which can effectively improve the voltage flip ratio for low quality factor of the resonant loop.

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References


