An improved segmented DAC for column readout circuit correction of large array CMOS image sensor

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Abstract The non-ideal factors and error sources of segmented DAC for multi-channel large array CMOS image sensor are given. An improved precise segmented DAC using adaptive switching technology is proposed. This scheme has been verified on a 50mm × 50mm large array CMOS image sensor prototype chip, which consisting of 8320 × 8320 pixel array was designed and fabricated in 55nm CMOS 1P4M standard process. The measurement results show that the DNL of DAC can be reduced from 33 LSBs of traditional structure to within 0.5LSB, and the large array sensor chip reaches a high intrinsic dynamic range of 75dB, a low FPN of 0.06%, and a low photo response non-uniformity of 1.5% respectively. Finally, a good raw image is taken by the prototype sensor.

Keywords: CMOS image sensor, column FPN, readout chain, DAC

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

With the development of CMOS technology and hybrid integration technology, CMOS image sensor (CIS) has become the most popular photoelectric conversion solid-state image sensor device [1, 2, 3, 4, 5]. Because CMOS image sensor has the characteristics of high integration, low power consumption and fast speed, the demand for CMOS image sensor is growing rapidly with the increasing application in recent years. At the same time, BSI and 3D stacked CMOS image sensors have high sensitivity and integration for small pixels [6, 7, 8, 9, 10, 11], which make up for the shortcomings of CCD and will further expand its application scope.

In scientific imaging, medical imaging and advanced machine vision image systems, CMOS image sensors require higher and higher resolution, array size and pixel number [12, 13, 14, 15, 16, 17, 18]. However, the large array will produce large parasitic resistance and capacitance, which will reduce the integration of the chip and the readout speed of the signal. Recently, several reports on high-speed CMOS image sensor have been published. An approach has been proposed in Ref. [19] in which all the column ADCs are fully utilized in both of the 2-to-1 and 3-to-1 subsampling modes, such that the maximum of 4× faster FHD and 9× faster HD videos are demonstrated with reference to the 1-to-1 non-subsampled 4K2K video. In Ref. [20], two sets of

60 channel column parallel pixel timing generator are placed at the top and bottom of the PCT-pixel array for providing even and odd pixel columns with timing control respectively. All of these will provide the effective solution for the speed problem, due to the large array and big image data. But it also suffers from the noise deterioration [21, 22], especially the Fixed Pattern Noise (FPN) because of the large layout area penalty [23, 24, 25, 26, 27, 28]. The signal data is transferred to the column processor and subtracted from the previously stored reset level data to provide FPN correction, designed in [29], which will occupy the readout cycle. A simple way to attenuate FPN in the three-FET APS operating in the wide-dynamic-range logarithmic mode was proposed in [30], which only requires the drain terminal of the reset transistor to be available. But it only deals with the pixel to pixel noise. At the same time, FPN will be further deteriorated with the urgent demand of science level and biological science for increasing the size of pixel array [31, 32].

In our previous work, investigation has been taken by the programming common voltage, adopting Digital to Analog Converter (DAC). Moreover, coarse conversion lay on the common area, and fine conversion lay on the individual channel is the superiority method to save the hardware cost. However, for high linearity and accuracy applications, existing nonlinear transformation at every transition point from upper to lower bit will be fatal to achieve good imaging quality. Therefore, the purpose of this paper is to realize high linearity DAC of large array CMOS image sensor for FPN and black level calibration.

2. Circuit architecture and implementation

The special feature of CMOS image sensor readout chain is that the layout of column circuit is fixed in a narrow pixel space, so the realization of column readout circuit needs to be simple. Due to the limited readout speed and stitching requirements of large-scale array, it is divided into multiple regions, resulting in the nonuniformity of multi channels. In particular, due to the mismatch of resistance, capacitance, gain and layout, there is also nonuniformity between even and odd columns of each channel. A common technique is to realize output feedback mechanism by programming DAC. Therefore, each channel will double the number of DACs to correct the column to column accuracy. To solve this problem, this paper proposes a reconfigurable DAC to deal with the deviation of multi channels, as shown in Fig. 1.

It is evidently the numbers of DAC will too much, which will occupy large layout area on the chip. This paper gives

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Fig. 1 reconfigurable DAC design diagram in multi-channels CIS

Fig. 2 nonlinearity in upper bit transition point

a method to solve the conflict through the separated high and low level range. For N bit DAC, Firstly high level is converted by the upper K bit DAC place the common system, which can be shared to the all DAC of channels. Secondly, low level is converted by the lower $N-K$ bit DAC place in the separate channel. The actual analog output is composed of the high and the low converter [33]. But there is a key problem, as shown in Fig. 2, which is the high order nonlinearity of turning point.

In the experiment, the whole chip is designed with eight channels, sixteen DACs are generated for correction, and sixteen high-level DACs are needed. To drive the long layout line, every high level DAC outputs two reference voltages through a buffer. When a column of data is output, switches s_1 and s_1' turn on in turn. The image data is output when the switch s_1 is on, and the reset data is output when the switch s_1' is on. Once the switch s_1 and s_{c1} is on, we can get the equation

$$Q_{C5} = C_5(V_{CM} + G(V_R - V_S) - V_{DAC1}) \quad (1)$$

$$Q_{C6} = 0 \quad (2)$$

Where V_{CM} is the column sampling common mode voltage, V_R is the reset voltage of pixel, V_S is the image voltage of pixel. Once the switch s_1' is on, s_{c1} is off, we can get the equation

$$Q_{C5}' = C_5(V_{CM} - V_{DAC}) \quad (3)$$

$$Q_{C6}' = \Delta Q_{C5} = C_5(V_{CM} + G(V_R - V_S) - V_{DAC1}) - C_5(V_{CM} - V_{DAC1})$$

Fig. 3 the separated high and low level range DAC diagram

$$= C_5 G(V_R - V_S) \quad (4)$$

So, the final output is

$$V_{OUT} = V_{DAC1} + G(V_R - V_S) \frac{C_5}{C_6} \quad (5)$$

This is the output result of odd columns of the first channel, and the other columns are the same process. It can be seen that the final output is adjusted by the DACs. Due to the inherent offset of 32 buffers and the buffer between channels, the linearity of the output reference voltage is poor, which leads to the large nonuniformity of CMOS image sensor. Assuming the offset of the buffers is V_{OS} , the first high level range is V_{H1} to V_{H2} , and the second high level range is V_{H3} to V_{H4} , as shown in Fig. 3. Because of the seamless turning, V_{H2} must be equal to V_{H3} , which is satisfied when the offset $V_{OS11} + V_{OS13}$ equals to $V_{OS12} + V_{OS14}$. As the layout of the upper buffer and the lower buffer is far away, in fact, the two offsets caused by the whole chain cannot be eliminated by the existing technology, so the nonlinearity inevitably occurs. Especially with the increase of pixel array size, the fixed pattern noise correction between channels becomes more and more urgent. However, the problem of upper bit transition jump of segmented DAC becomes very serious.

$$V_{OS1} = V_{OS11} + V_{OS13} \quad (6)$$

$$V_{OS2} = V_{OS12} + V_{OS14} \quad (7)$$

$$V_{H1} = V_{RL} + V_{OS11} + V_{OS13} \quad (8)$$

$$V_{H2} = \frac{V_{RH} - V_{RL}}{2^K} + V_{OS12} + V_{OS14} \quad (9)$$

$$V_{H3} = \frac{V_{RH} - V_{RL}}{2^K} + V_{OS11} + V_{OS13} \quad (10)$$

$$V_{H4} = \frac{V_{RH} - V_{RL}}{2^{K-1}} + V_{OS12} + V_{OS14} \quad (11)$$

To solve the above problems, a novel segmented DAC structure is proposed as shown in Fig. 4. For the first section, the low reference voltage of the lower $K-M$ bit V_{H1} is transformed by the switch 70, sharing buffer 30, switch 110 and local buffer 301. Meanwhile, the high reference voltage of the low $K-M$ bit V_{H2} is transformed by the switch 50, sharing buffer 20, switch 90 and local buffer 201. For the second section, the low reference voltage of the low $K-M$ bit V_{H3} is transformed by the switch 50, switch 90 and local buffer 201 under the same signal line as

Fig. 4 proposed segmented DAC structure with adaptive signal chain switch technique

Fig. 5 Die micrograph

the low reference in first section. The high reference voltage of the low K-M bit V_{H4} is transformed by the switch 70, sharing buffer 30, switch 110 and local buffer 301 under the same signal line as the high reference in first section. Similarly, for the third section, the low reference voltage of the lower K-M bit V_{H5} is transformed by the switch 70, sharing buffer 30, switch 110 and local buffer 301, the high reference voltage of the low K-M bit V_{H6} is transformed by the switch 50, sharing buffer 20, switch 90 and local buffer 201. Through the dynamic switching of the transformation chain, all the offsets caused by buffers and lines are eliminated completely.

3. Experiments and results

A prototype image sensor chip is implemented in a 55nm CMOS image sensor technology. The die micrograph of the fabricated sensor is shown in Fig. 5, which consists of an 8320×8320 pixel array and peripheral circuitry. Column parallel DAC arrays are located on a single side located below the pixel array. In order to improve the frame rate and meet the stitching process requirements. The whole chip is divided into eight channels, and the odd and even columns of the same channel are also separated. So thirty two DACs of ten bit are designed in this project, and the high level is converted by the shared four bits, the low level is converted by the local six bits in the channel. Therefore, the resistor strings is reduced from 2^{10} to $2^4 + 2^6$, greatly reducing the layout area. The poor DNL is shown in Fig. 6, the results under pre-calibration is about 33LSB. With the proposed calibration, the excellent DNL under post-calibration can be easily reduced to 0.5LSB, and the column FPN and black

Fig. 6 DNL under pre-calibration and post-calibration

Fig. 7 Gray value statistics of different channels under without/with calibration

Table I Characteristics summary of test chip

Technology	55nm 1P4M
Chip size	50mm×55mm
Numbers of pixel	8320×8320
Supply	3.3V/1.2V
Pixel size	5.7μm
Fill Factor	57.4%
Effective Peak Quantum efficiency	55%
Swing range	1.5V
PRNU	1.5%
Column FPN	0.06%
Read noise	< 5e-
Dynamic range(intrinsic)	75dB

level can be corrected very accurately.

There is an obvious column FPN in the multi channels under without calibration, as shown in the blue curve in Fig. 7. According to the actual test results, we can get the deviations of the eight channels in the prototype image sensor. Then compensation is transferred to the internal register by the SPI configuration. Therefore, the results after calibration are shown in the red curve in Fig. 7. Fig. 8 shows the prototype camera and the original sample image using the sensor chip of this paper. Despite increasing large chip size is up to $50\text{mm} \times 55\text{mm}$, it still remains at a low level of $5e^-$ read noise, 0.06% column FPN, and a wide intrinsic dynamic range of 75dB. Finally, specifications and characteristics are summarized in Table I.

Fig. 8 Prototype camera and raw image

4. Conclusion

An improved segmented DAC with high linearity and accuracy in multi-channels large array CMOS image sensor is proposed in this paper. The common mode level between channels and between odd and even columns can be precisely controlled to compensate for the column FPN and black level caused by circuit mismatch and dark current. At the same time, it can keep a perfect match with the common mode level of the successive ADC input, so as to maximize the intrinsic dynamic range of the system. Finally, a high intrinsic dynamic range, low column FPN and black level CMOS image sensor chip prototype composed of 64M 4T active pixel sensor array is designed and fabricated by using 55nm CMOS 1P4M standard technology. The measured results achieved a DR of 75 dB, a FPN of 0.06%, and a PRNU of 1.5% respectively. Good original image is obtained by the prototype sensor, which proves that the improved segmented DAC is successfully implemented.

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