Design and analysis of monolithic triple-stacked power amplifiers using GaAs HBT-HEMT process

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Abstract This paper describes design and analysis of monolithic triple-stacked power amplifiers (PAs) in 2- μm / 0.5- μm GaAs HBT-HEMT process. The proposed PAs are designed using both heterojunction bipolar transistor (HBT) and high electron-mobility transistor (HEMT). Based on a common-emitter (CE) configuration of HBT with stacked common-gate (CG) configuration of HEMTs or stacked common-base (CB) configuration of HBT as the third-stacked transistor, better power performances with good PAEs can be achieved as compared with the CE or common-source (CS) amplifier due to high output stacking impedance. The bandwidth with HEMT/CG configuration as the third-stacked transistor is investigated. The proposed stacked PAs demonstrate a maximum output powers of 31.7 dBm, a compact chip size of within $1.6 \times 1 \text{ mm}^2$, and a maximum power added efficiency (PAE) of 38.3% at 5 GHz.

Keywords: GaAs, heterojunction bipolar transistor (HBT), high electron-mobility transistor (HEMT), microwave circuits, monolithic microwave integrated circuit (MMIC), power amplifier (PA)

Classification: Microwave and millimeter-wave devices, circuits, and modules

1. Introduction

Stacked transistor is widely used in several radio frequency (RF) circuits. Based on the voltage multiplication, the output power can be enhanced with high output impedance for the power amplifier (PA) design [1]. For the conventional stacked PA, a common-source (CS) transistor is used to drive a common-gate (CG) transistor. With a proper gate termination, the output power can be enhanced by the maximum power of each transistor. For the conventional n -stacked PA, the stacked transistors are all designed using the same type transistor, such as HBT [2, 3, 4, 5, 6, 7, 8, 9, 10], NMOS [11, 12, 13, 14, 15, 16, 17, 18] and high electron-mobility transistor (HEMT) [19, 20, 21, 22]. A broadband monolithic GaAs heterojunction bipolar transistor (HBT)-HEMT/common-emitter (CE) and common-gate (CG) stacked PA has been proposed in [23]. Based on a CE transistor stacked with a CG transistor, the wide bandwidth and high output power can be achieved. The monolithic HBT-HEMT process offers great design flexibility to achieve superior performance. To date, a frequency quadrupler [24], distributed amplifiers [25, 26], a frequency tripler [27], voltage-controlled oscillators [28, 29], and a variable gain

amplifier [30] have been presented using several advanced HBT-HEMT processes.

In this paper, two PAs are designed using a triple-stacked topology. Based on the CE-CG configuration with two different stacked transistors, the proposed triple-stacked PAs perform watt-level high output power. The device selection and optimal capacitance of gate terminal capacitor are presented. For broadband and high output power performance, the triple-stacked PA using CE-CG-CG (Type-I) configuration with stacked depletion-mode (D-mode) HEMT is used. The input and output matching networks are also designed to achieve broad bandwidth. The proposed PAs feature a maximum output powers of higher than 30 dBm, a maximum power added efficiency (PAE) of 30%, and a compact chip size of within $1.6 \times 1 \text{ mm}^2$. As compared to the PA in [23], the proposed stacked PAs are designed using CE-CG-CG (Type-I) and CE-CG-CB (Type-II) triple-stacked topologies. The Type-II PA is designed to compare with the Type-I PA. The bandwidth and output power are investigated. The design methodology of triple-stacked PAs using the HBT-HEMT process is presented with theoretical calculation. With a stacked CG HEMT transistor in triple-stacked PA, the higher output power can be achieved with good efficiency.

2. Stacked transistor selection and capacitance design

The proposed triple-stack PAs are designed using the GaAs HBT-HEMT process provided by the WIN Semiconductors Corporation, Taiwan. The breakdown voltages of the HBT and HEMT are 15 and 20 V, respectively. The unity current gain frequencies (f_T) are higher than 35 and 40 GHz for HEMT and HBT, respectively. The maximum oscillation frequencies (f_{max}) are higher than 100 and 70 GHz for HEMT and HBT, respectively. The schematics of the proposed triple-stacked PAs are shown in Fig. 1. The triple-stacked PA is composed of one CE transistor with two stacked CG (or CB) transistors. The output power of n -stacked PA can be expressed as [23]

$$P_{\text{out}} = n^2 \frac{(V_{ds} - V_k)^2}{2R_{\text{opt}}} = \frac{n}{2} I_d^2 R_L, \quad (1)$$

where n is 3 for our proposed PAs, R_{opt} , R_L , V_{ds} , V_k , and I_d are the optimum output load impedance, load impedance of stacked transistor, drain-to-source voltage, knee voltage, and dc supply current, respectively. R_{opt} is

$$R_{\text{opt-PA}} = nR_L = n \frac{\Delta V}{\Delta I} = n \frac{V_{ds} - V_k}{I_d} \quad (2)$$

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Fig. 1 Schematics of the proposed (a) Type-I, and (b) Type-II triple-stacked PAs.

Fig. 2 Equivalent CG (or CB) circuit of the stacked transistor.

Table I Device characteristics of the transistors.

Device	g_m (S)	$C_{be}(C_{gs})$ (pF)	R_L (Ω)	V_k (V)	C_{g3} (pF)	Z_{in}
HBT	0.082	0.28	17.5	0.57	0.6	17.9
D-mode HEMT	0.151	1.2	16.3	0.81	0.74	17.4
E-mode HEMT	0.291	1.4	15.1	1.04	0.4	15.5

where R_L is the load impedance of each stacked transistor. From (2), R_{opt_PA} increases with R_L . Since the dc currents (I_d) across each transistor of the stacked PA are all the same, the output power can be enhanced by stacking the transistor. The optimum output impedance has been addressed in [23]. The input impedance looked into the source of the equivalent circuit in Fig. 2 can be expressed as

$$Z_{in} = \frac{1}{g_m} \left[1 + \frac{C_{gs}}{C_{g2}} - \omega^2 L_g C_{gs} + j\omega R_g C_{gs} \right] \quad (3)$$

where g_m , C_{gs} (C_{be}), and C_{g2} are the transconductance, gate-to-source (base-to-emitter) capacitance, and gate termination capacitance, respectively, for Q_2 in Fig. 1. R_g and L_g are parasitic resistance and inductance. The maximum output power can be estimated using (1) and (2) from V_{ds} , V_k , and R_L of each transistor. The device characteristics of the HBT-HEMT process, including HBT, E/D-mode HEMTs, are summarized in Table I with a V_{ds} (or V_{ce}) of 4 V. Both stacked PAs are with a dc supply voltage (V_{dd}) of 12 V, and an I_d of 196 mA. The V_k , and R_L of each transistor are shown in Table I. The simulated current is 196 mA to achieve the maximum output power of 30 dBm. The maximum output power and the increment of output power versus stacked number (n) are shown in Fig. 3. As compared to the conventional CE (or CS) amplifier, the output power of the proposed stacked PA with a stacked number (n) of 2 has the

Fig. 3 Simulated maximum output power and increment of maximum output power versus stacked number (n).

Fig. 4 Simulated normalized capacitance ratio of C_{gs}/C_{g2} and C_{be}/C_{g2} versus frequency.

best improvement of output power up to 3 dB. The output power increases as the stacked number (n) increases, but the improvement of output power decreases. To have the best stacked efficiency with large output power, n is 3 for the proposed stacked PAs.

From (3), the input impedance (Z_{in}) of the stacked transistor is varying with the capacitance ratio of C_{gs}/C_{g2} , and the phase of the input impedance (Z_{in}) is also affected by the capacitance ratio. In order to achieve broad bandwidth, the matching between the R_{opt} and R_L should be properly designed. Since the C_{gs}/C_{be} of the simple equivalent circuit in Fig. 2 is varying with the dc bias, RF power, and frequency, the impedance, Z_{in} , is affected. The output bandwidth of the stacked PA is affected by the phase of Z_{in} . The simulated normalized capacitance ratio C_{gs}/C_{g2} or C_{be}/C_{g2} versus frequency is plotted in Fig. 4. The simulated normalized capacitance ratio C_{gs}/C_{g2} for the stacked transistor using depletion-mode (D-mode) HEMT features the widest frequency response, and therefore the stacked PA using the HBT-HEMT(D)/CE-CG configuration has potential to demonstrate the broad bandwidth.

To enhance the maximum output power with good efficiency, the triple-stacked PAs are designed and implemented. For the simulated results, the capacitance of C_{g2} and C_{g3} should be properly selected based on the dynamic load lines of Q_2 and Q_3 . To achieve the maximum output power, the stacked transistors (Q_2 and Q_3) should have the largest voltage swing between the drain and the source. The

Fig. 5 The simulated voltage swings for the Type-I and Type-II configurations: (a) between node “A” and ground with an input power of 22 dBm, (b) between nodes “B” and “A” with an input power of 22 dBm, (c) between nodes “C” and “B” with an input power of 22 dBm.

large voltage swings of the PAs can be achieved with proper capacitances of C_{g2} and C_{g3} , as well as the optimum load impedance. In Fig. 2, C_{g2} performs a capacitive voltage divider and produces the proper in-phase voltage swing at the gate and drain. For the triple-stacked PA design, the most critical parameter is the capacitance of C_{g2} and C_{g3} due to the output power. Moreover, the HEMT is more suitable for the upper transistor of the stacked PA since the HEMT has larger breakdown voltage than the HBT (higher than 5 V). The voltage swing across nodes “B” and “A” in Fig. 1 is affected by the third-stacked transistor. As compared to the enhancement-mode (E-mode) HEMT, the D-mode is more suitable for the stacked transistor, since the knee voltage of the D-mode HEMT is lower than the E-mode HEMT and results in larger voltage swing.

Based on the HBT-HEMT(D)/CE-CG dual-stacked PA performance, the third-stacked transistor of triple-stacked PA is designed to enhance the output power with high efficiency and broad bandwidth. The simulated voltage swings between node “A” and ground, between nodes “B” and “A”, and between nodes “C” and “B” in Fig. 1 are plotted in Fig. 5 for the HBT-HEMT(D)-HEMT(D)/CE-CG-CG (Type-I) and HBT-HEMT(D)-HBT/CE-CG-CB (Type-II) configurations. To make fair comparison between the two PAs, the input powers are 22 dBm in Fig. 5. As can be observed, the voltage swing across the second-stacked transistor of the Type-I configuration is higher than the Type-II configuration. Although the voltage swing at the third-stacked transistor of the Type-I configuration is higher than the Type-II for most of the period, the voltage swings at the third-stacked transistor of the Type-II configuration is much higher than the Type-I as shown in Fig. 5(b) and (c). In addition, the gate dc bias of the stacked transistor can also be lowered since the gate-to-source voltage of the D-mode HEMT is negative. The simulated insertion phases between nodes “C” and “B” for the stacked HBT and HEMT transistors with the gate capacitances are shown in Fig. 6. As can be observed, the stacked transistor of HEMT(D) has wider frequency response than the HBT. Therefore, the Type-I configuration is more suitable for the triple-stacked PA design in the GaAs HBT-HEMT technology due to its high maximum output power and wide bandwidth performance.

Fig. 6 The simulated insertion phases between nodes “C” and “B” in Fig. 1 for the Type-I (stacked HEMT) and Type-II (stacked HBT) configurations.

3. Circuit design and power amplifier implementation

To verify the proposed design concept, two stacked PAs are implemented using GaAs HBT-HEMT process. The schematics of the proposed triple-stacked PAs are shown in Fig. 7. Since the n -stacked amplifier has n times of the load impedance R_L , the output impedance of the stacked amplifier should be close to the system impedance (Z_0) as compared to the conventional CS (or CE) amplifier, especially for the large device size. Therefore, the output matching network can be designed using 2-section LC network in the region of low Constant- Q (Q_n) contour to achieve broad bandwidth. The termination networks C_{g2} and C_{g3} are designed using (3). The emitter area of Q_1 is $1080\mu\text{m}^2$, and the total gate width of Q_2 is $2400\mu\text{m}$. Since the overall current of the stacked PA is limited by the Q_1 , the sizes of the third-transistors are chosen to be the same as Q_1 and Q_2 to make sure that Q_3 , Q_2 , and Q_1 have the same dc performance. For the Type-I triple-stacked PA, the total gate width of Q_3 is $2400\mu\text{m}$. For the Type-II triple-stacked PA, the emitter area of Q_3 is $1080\mu\text{m}^2$. The device size selection and R_{opt} is simulated using load-pull setup. In order to match a $50\text{-}\Omega$ load to the optimum load impedance R_{opt} , 2-section LC elements (L_5 , L_6 , C_5 , and C_6) are designed for the output matching network with a Q_n of within 1 for the Type-I configuration. Since the R_{opt} of Type-II configuration is higher than the Type-I configuration, 1-section LC elements (L_5 , L_6 , and C_6) are designed for the output matching. For

Fig. 10 Simulated and measured results at 5 GHz: (a) output powers, gains, and PAEs for the Type-I triple-stacked PA, and (b) output powers, gains, and PAEs for the Type-II triple-stacked PAs.

Fig. 7 The schematics of the proposed Type-I and Type-II triple-stacked PAs.

Fig. 8 Chip photos of the (a) Type-I, and (b) Type-II triple-stacked PAs with chip sizes of $1.6 \times 1 \text{ mm}^2$ and $1.5 \times 1 \text{ mm}^2$.

the input matching network, the 3-section LC elements (L_1 , L_2 , L_3 , C_1 , C_2 , C_3 , and C_4) are employed for the input matching network with a Q_n of within 1.6 to widen 3-dB gain bandwidth of the stacked PAs. The dc current source is designed as the bias circuit at the base terminal of HBT/CE transistor to stabilize the dc bias [23].

The chip photos of the Type-I and Type-II triple-stacked PAs are shown in Fig. 8. The chip sizes are $1.6 \times 1 \text{ mm}^2$, and $1.5 \times 1 \text{ mm}^2$ for the Type-I and the Type-II triple-stacked PAs, respectively. The transistors are biased at saturation region for HEMT and active region for HBT. The RF performances are measured via on-wafer probing. The simulated and measured large-signal gains with an input power of 5 dBm are shown in Fig. 9 for the Type-I and the Type-II triple-stacked PAs. The measured large-signal gain of the Type-I triple-stacked PA for $V_{g2} = 3.6$ and $V_{g3} = 10 \text{ V}$ is higher than 10 dB from 3 to 6 GHz. The measured large-signal gain of the Type-II triple-stacked PA for $V_{g2} = 3.6$ and $V_{g3} = 15 \text{ V}$ is higher than 10 dB from 3.5 to 5 GHz. The simulated and

Fig. 9 Simulated and measured large signal gains, input and output return losses of the triple-stacked PAs, (a) Type-I, and (b) Type-II, where the input power (P_{in}) is 5 dBm.

measured output powers, and PAEs versus input power with a dc supply voltage V_{dd} of 12 V are shown in Fig. 10 for the Type-I and the Type-II triple-stacked PAs. The measured output 1-dB compression points (P_{1dB}) are 29.6 dBm and 29.7 dBm for the Type-I PA and the Type-II triple-stacked PAs, respectively. The measured maximum PAE for the Type-I and the Type-II triple-stacked PAs is 38.3% and 30.6%, respectively. Both of the proposed PAs can achieve the maximum output power of higher than 30 dBm. The proposed Type-I triple-stacked PA has wider bandwidth and higher maximum output power than the Type-II configuration. The experimental results agree well with the discussion in Section 2. The linearity characteristics of the

Table II Performance comparison of the previously reported stacked power amplifiers and this work.

Ref.	Topology	DC (V)	Freq. (GHz)	Bandwidth (%)	Gain (dB)	P _{1dB} (dBm)	P _{sat} (dBm)	PAE (%) (P _{1dB} /P _{sat})	FOM	Fully Integrated	Process
[14]	2-stage	2.4 (driver)	47	-	24.9	-	20.1	- / 15.6	70.4	Yes	45 nm SOI CMOS
	4-stacked	4.8	47.5	40	12.8	-	20.3	- / 19.4	59.5	Yes	
[16]	2-stacked	6	0.1-6.5	193	18.4 ±1.5	18-19	22	- / 17	48.3	Yes	0.18 μm CMOS process
[17]	3-stacked	2.8	25-30.5	20	9.9	14.9	18.8	- / 23.4	31.3		22 nm SOI CMOS
[18]	3-stack	3.6	38	-	17.5	14.8	17.3	- / 24.3	39.8	Yes	65 nm CMOS
[19]	4-parallel 3-stacked	15	4-10	85.7	13.5 ±1.5	-	35-37	- / 25-32	67.6	Yes	0.15 μm GaAs HEMT
[23]	2-stacked CE-CG	8 12	3.5-6.5 3.5-6.5	60 60	13.5 11	26.4 29.1	27 29.4	35.6 / 38 28.5 / 27.2	50.3 48.7	Yes	2 μm / 0.5 μm GaAs HBT-HEMT
	3-stacked CE-CG-CG	12	3.1-5.8	60.6	15.7 9.9*	29.57	31.67	28.8 / 38.3	57.2 51.4*	Yes	2 μm / 0.5 μm GaAs HBT-HEMT
This work	3-stacked CE-CG-CB	12	3.3-5.6	51.7	14.9 8.4*	29.7	30.5	30.5 / 30.6	54.2 47.8*	Yes	

*small signal gain

triple-stack PAs are measured using continuous-wave (CW) two-tone signals with a frequency spacing of 2 MHz, and the central frequency is 5 GHz. The measured third-order IMDs (IMD3s) of Type-I and Type-II PAs are 30 dBc with an input power of 8.5 dBm. To evaluate the circuit performance of the previously reported stacked PAs and this work, a figure-of-merit (FOM) is defined as [14]

$$\text{FOM} = P_{\text{sat}} + G + 10 \log_{10} \text{PAE} + 20 \log_{10} f_0 \quad (4)$$

where P_{sat} is the saturated output power in dBm, G is the power gain in dB, and f_0 is the center frequency in GHz. Table II shows the performance comparison of the previously reported stacked PAs and this work. Our proposed triple-stacked PAs perform high maximum output power with good PAE. As compared the bandwidth to [16], the bandwidth of the PA in [16] is wider than the proposed PAs, due to the used of external bias-tee network. Although the bias-tee achieves broadband frequency response at the output, the cost of the PA increases. As compared to the PA in [23], the proposed triple-stacked PAs have better PAEs at output $P_{1\text{dB}}$, and better output saturated power (P_{sat}) than the dual-stacked PA with a dc supply voltage V_{dd} of 12 V. With the HEMT(D)/CG as the third-stacked transistor, the maximum output power is enhanced with good PAE. The CE-CG-CG configuration triple-stacked PA also has the same bandwidth as the CE-CG compared to the dual-stacked PA in [23].

4. Conclusion

Two monolithic triple-stacked PAs using a 2-μm/0.5-μm GaAs HBT-HEMT process are successfully presented in this paper. Based on a CE-CG configuration with stacked CG and CB configurations, the proposed triple-stacked PAs demonstrate high output power and broad bandwidth. The proposed CE-CG-CG triple-stacked PA has wider bandwidth than the CE-CG-CB configuration. It can be further utilized for the modern mobile applications due to its good circuit performance and the mass-production MMIC process.

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