LETTER

An optimized fully-passive noise-shaping SAR ADC with integration capacitor reuse technique

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Abstract This paper presents an optimized Fully-Passive Noise-Shaping Successive Approximation Register (FPNS-SAR) Analog-to-Digital Converter (ADC) with passive gain and integration capacitor reuse techniques. Instead of using multi-input-pair comparator with active gain in traditional Cascaded Integrator Feed-Forward (CIFF) structure, 1-input-pair comparator with passive gain is adopted in this paper to reduce power consumption and kick-back noise. The proposed FPNS-SAR ADC was implemented with standard 65-nm CMOS process. With the oversampling ratio (OSR) of 8, the simulation results realize 79.3 dB peak SNDR and 94 dB peak SFDR at 6.25 MHz input signal bandwidth and 100 MHz sampling frequency. The proposed ADC consumes 1.245 mW at 1.2 V supply voltage. The calculated FOMw and FOMs are 13.2 fJ/conv.-step and 176.3 dB, respectively.

Keywords: Analog-to-Digital Converter (ADC), Fully-Passive Noise-Shaping (FPNS), Cascaded Integrator Feed-Forward (CIFF), Successive Approximation Register (SAR)

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

The Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) is widely used in moderate resolution and conversion rate due to its structure simplicity, low power consumption and friendly for process scaling. Due to the limitation of the quantization noise and thermal noise, the resolution of SAR ADC can only achieve about 10-bit [1, 2]. Refs. [3, 4, 5, 6] had achieved a resolution greater than 12-bit with extra calibration circuit, but resulting more power consumption and lower conversion rate. In addition, the oversampling and noise shaping techniques implemented in sigma-delta ADC [7] are the effective ways to improve conversion accuracy. Nevertheless, the traditional Operational Transconductance Amplifier (OTA) based sigma-delta ADC [8, 9, 10, 11] is not a good choice in low power consumption application. To address these challenges, Ref. [12] and [13] had proposed VCO-based quantizer Sigma-Delta ADC to decrease the power consumption. However, the linearity of the VCO is sensitive to the vibration of Process Voltage-Temperature (PVT).

Recent researches had brought forward an attractive solution, the noise-shaping SAR (NS-SAR) ADC, which combines the oversampling and noise-shaping techniques with

SAR ADC [14, 15, 16, 17, 18, 19, 20, 21, 22, 23]. The active noise-shaping technique proposed in Refs. [14, 15, 16] is implemented by OTA to integrate the residue voltage, which sacrifices power efficiency and scaling compatibility to achieve a better noise transform function (NTF). Without OTA based integrator, Refs. [17, 18, 19] adopt Dynamic Amplifier (D-Amp) to cut down power consumption while maintaining noise suppression in-band simultaneously. However, they are very sensitive to PVT vibration, resulting in poor robust. Refs. [20, 21, 22, 23] has designed several fully-passive switch capacitor integrators, mainly including Cascaded Integrator Feed-Forward (CIFF) and Error-Feedback (EF) structures. As shown in Fig. 1, an active gain multiple input comparator is required in traditional CIFF NS-SAR to compensate for residual voltage loss, but it will generate additional power consumption and input-referred noise.

To address those issues, the passive gain and integration capacitor reuse techniques are introduced in the proposed fully-passive noise-shaping SAR ADC. Compared with traditional CIFF structure, the proposed design reduces the power consumption and kick back noise of the comparator, while retaining the strong noise-shaping effect simultaneously. The optimized FPNS SAR realizes 1st-order noise shaping effect and its NTF can achieve 19 dB in-band attenuation. Designed in 65-nm CMOS process, it obtains 79.3 dB SNDR with 10-bit Capacitive Digital-to-Analog Converter (CDAC) array. Additionally, the body effect cancellation technique is applied in bootstrap sampling switch to enhance linearity.

The rest of this paper is organized as follows. The architecture of the proposed optimized fully-passive noise-shaping SAR ADC and its conversion process are described in Section 2. The circuit implementation details are shown in Section 3. The simulation results are presented in Section 4. Finally, a conclusion is drawn in Section 5.

Fig. 1 The block diagram of the traditional CIFF NS-SAR.

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2. Proposed FPNS-SAR

The architecture of the proposed fully-passive noise-shaping SAR ADC and its time diagram are shown in Fig. 2, which is mainly composed of the CDAC array, the passive switch-capacitor integrator, the comparator and the SAR logic. Although the actual CDAC array is fully differential, for simplicity, a single-ended version is drawn here.

In the sampling phase of φ_s , the top plates of the CDAC array are connected to the input signal, while the bottom plates are reset to V_{cm} . In the course of conversion, the SAR ADC carries out successive comparison which performs V_{cm} -based switching capacitor procedure to guarantee the common voltage of the differential input V_{in} and V_{ip} constant [24].

After the conversion phase of φ_c , the residual voltage V_{res} is generated by returning the LSB's decision to the CDAC array, which is boosted twice by passive gain technique. Fig. 3 demonstrates the process of the CDAC to achieve passive gain, where C_{MSB} is the most significant capacitance and the C_{LSB} represents all the remaining capacitance.

Fig. 4(a) shows the conversion process of the 1st-order noise-shaping performed by the passive switch-capacitor filter in the integration phase φ_1 and its single-ended equivalent circuit is shown in Fig. 4(b). Due to the charge redistribution between the CDAC capacitor and the integration capacitor, the residual voltage V'_{res} changes as described in Eq. (1).

$$4CV_{int}(n-1) + CV'_{res}(n) = 5CV_{int}(n) \quad (1)$$

Where C is the total capacitance of the CDAC. The expression in z-domain is shown in Eq. (2).

$$V_{int}(z) = \frac{0.2}{1 - 0.8z^{-1}} V'_{res}(z) \quad (2)$$

Fig. 2 Architecture of the proposed FPNS-SAR and its time diagram.

Fig. 3 Passive gain of the CDAC.

The 1st-order noise-shaping is completed. In the next conversion phase of φ_c , the integrated residual voltage $V_{int}(z)$ will be boosted to 4 times through capacitor passive addition method. Meanwhile, the voltage of the comparator input equal to $V'_{res}(n) + 4V_{int}(n)$. Compared to 2-input-pair, the power consumption of the comparator has been cut down by using passive addition method. The equivalent circuit of the integrated capacitor reuse technique is illustrated in Fig. 5.

The signal flow diagram of the proposed FPNS-SAR is shown in Fig. 6. Based on Eq. (2), the passive integration function can be expressed as

$$H(z) = \frac{0.2}{1 - 0.8z^{-1}} \quad (3)$$

From the signal flow diagram, the expression of the digital output has been calculated.

$$D_{out}(z) = V_{in}(z) + 4V_{int}(z) + Q(z) \quad (4)$$

By analyzing the signal flow diagram and combining with Eq. (4), the transfer function of the proposed FPNS-SAR can be expressed as

$$D_{out}(z) = V_{in}(z) + \frac{1 - 0.8z^{-1}}{1 + 0.8z^{-1}} Q(z) \quad (5)$$

From Eq. (5), the noise transform function can be calculated as

$$NTF(z) = \frac{1 - 0.8z^{-1}}{1 + 0.8z^{-1}} \quad (6)$$

Fig. 4 The 1st-integration process.

Fig. 5 The passive addition and integration capacitor reuse.

Fig. 6 General signal flow diagram of the proposed FPNS SAR ADC.

Fig. 7 Bode-diagrams comparison in this paper and prior works.

Fig. 8 Implementation of the bootstrap switch.

which contains one zero located in $z = 0.8$ and one pole located in $z = -0.8$. The bode-diagrams comparison in this paper and prior works, shown in Fig. 7, proves that the NTF of the proposed FPNS-SAR can achieve 19 dB noise attenuation in signal band.

3. Circuit implementation

3.1 Bootstrap switch

The performance of the sample and hold circuit is critical for high-speed and high-precision ADCs. General NMOS switch and CMOS transmission gate are not good choices for those application with low nonlinear distortion. To reduce harmonic distortion, the bootstrap switches are adopted in ADCs [25, 26]. However, the linearity of the bootstrap switch is mainly deteriorated by the charge injection effect and body effect. In a fully differential SAR ADC, the charge injection can be eliminated by differential sampling. In order to solve the body effect, the structure of the bootstrap switch with bode effect cancellation technique is shown in Fig. 8.

$$R_{on} = \frac{1}{\mu_n C_{ox} (W/L) (V_{GS} - V_{th})} \quad (7)$$

The calculated equivalent on-resistance of the switching transistor, R_{on} , is shown in Eq. (7). Due to the variable V_{th} caused by body effect, the nonlinearity of the sampling switches gets worse. In this work, transistors M10, M11 and M12 are added to the bootstrap circuit to keep V_{th} constant, thereby eliminating the nonlinearity.

To verify the effectiveness of this technique, Fig. 9(a) and Fig. 9(b) show the sampling signal spectrum of before body effect cancellation and after body effect cancellation, respectively. From the FFT results, the dynamic performance

(a) Before body effect cancellation

(b) after body effect cancellation

Fig. 9 Body effect cancellation technique in bootstrap switch.

Fig. 10 The double-tail comparator.

Fig. 11 Generation circuit of f_{clk} .

can be significantly improved with body effect cancellation technique under the condition of 8 MHz input sine wave and 125 MHz sampling rate. After body effect cancellation, the SNDR and SFDR increase by 5 dB and 7.5 dB, respectively.

3.2 Clock generation circuit

Asynchronous sequential logic is used in the SAR ADC [1, 24] to improve the conversion rate, which reduces the requirements of the external clock and thereby the overall power consumption of the circuit.

The clock generation circuit works like an oscillator and is mainly composed of a comparator and 3-input NAND gate. As depicted in Fig. 10, the double-tail dynamic comparator controlled by f_{clk} is adopted in this work to reduce the power consumption and kick-back noise of the comparator [27].

Fig. 11 shows the overall circuit implementation of the internal clock. Where, the RDY signal is the conversion completion signal, while Outp and Outn are the output sig-

Fig. 12 Simulated FFT spectrum at 100 MHz.

Fig. 13 Simulated SNDR versus (a) input amplitude and (b) OSR.

nals of the comparator.

4. Results and discussion

The proposed optimized FPNS SAR was designed in TSMC 1P8M 65-nm CMOS technology. The minimum MIM capacitance defined by this process is 9.4 fF with an area $2\text{ }\mu\text{m} \times 2\text{ }\mu\text{m}$. The unit capacitance used in this paper is 4.7 fF, which is realized by two minimum process-defined MIM capacitors connected in series. With 1.2 V supply voltage and 100 MHz sampling frequency, the total power consumption is 1.245 mW.

Fig. 12 demonstrates the 16384-point Fast Fourier Transform spectrum of this work with a -1 dBFS sine wave at 500 KHz. The bandwidth of the input signal is 6.25 MHz with an OSR of 8. From the measured spectrum, the ADC achieves a peak SNDR of 79.3 dB and a peak SFDR of 94 dB with 1st-order noise shaping. Furthermore, an ENOB of 12.88 bits was achieved with a 10-bit CDAC array.

Fig. 13 illustrates the simulated SNDR versus the input amplitude and the OSR. The performance comparison with

Table I Performance summary and comparison.

Architecture	Ref[14]* JSSC'12	Ref[19]* IEICE'18	Ref[21]* VLSI'17	Ref[30]** VLSI'18	This work**
	Active NS SAR	D-Amp NS SAR	FPNS SAR	FPNS SAR	FPNS SAR
Technology (nm)	65	65	40	65	65
Supply (V)	1.2	1	1	1	1.2
Sampling rate (MS/s)	90	25	8.4	100	100
OSR	4	20	16	25	8
Bandwidth (MHz)	11	0.625	0.26	2	6.25
SNDR (dB)	62.14	80.4	80	82	79.3
Power (uW)	806	630.2	140	561	1245
FoMs (dB)	163.5	170.4	173	176	176.3
FoMw (fJ/conv.step)	35.8	59	33	16	13.2
FOMs = SNDR (dB)+10lg (BW/Power)					
FOMw = Power/2 ^{ENOB} *2*BW					

*: measured

**: simulation

the prior works is presented in Table I [30].

5. Conclusion

To further reduce the overall power consumption of the ADC while maintaining good noise shaping effect, an optimized FPNS SAR ADC with passive gain and integration capacitor reuse techniques was proposed in this paper. It achieves a peak SNDR of 79.3 dB and a peak SFDR of 94 dB at 100 MHz sampling frequency. Compared with prior works, a better noise-shaping effect has been realized in CIFF structure which requested only 1-input-pair comparator. Meanwhile, the body effect cancellation bootstrap switch is also adopted in this paper to achieve better linearity.

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