A modified pulse swallow frequency divider for fractional-N PLL

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Abstract A modified pulse swallow frequency divider for fractional-N frequency synthesizers was designed and implemented in a 0.18 μm CMOS process. The proposed structure inserts a pulser between D flip-flop 1 (DFF1) and B counter to solve the possible malfunction of the SR latch and the unwanted division ratio offset in the conventional structure. To remarkably improve the operating speed, a D flip-flop 2 (DFF2) was employed to retiming the modulus control (MC) signal. The proposed frequency divider can work at an input clock signal frequency up to 7.04 GHz with a power consumption of only 7.59 mW.

Keywords: frequency divider, pulse swallow counter, fractional-N frequency synthesizer

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

The design of fractional-N frequency synthesizer has become a popular research field. Fractional-N frequency synthesizer has been widely and successfully used in devices that require high precision frequency sources, such as global navigation satellite system (GNSS) RF receiver, high-precision base stations, and mobile phone RF transceiver chips, etc. As a crucial component of the fractional-N frequency synthesizer, the frequency divider puts forward higher requirements. Therefore, a high operating speed and low power consumption fractional-N frequency divider are highly desired [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20]. The working speed limitation of pulse swallow frequency divider is determined by the delay time of MC signal (τ_{MC}) [1, 2, 3, 20, 21, 22, 23, 24, 25, 26]. In [1], a D flip-flop was adopted to retiming the MC so as to reduce τ_{MC} . While, this structure inherently possesses an unwanted division ratio offset of one because the MC signal's set and reset were triggered by different signals. To solve this problem, MC signals were triggered by a single signal in [2, 3]. However, these two architectures lead to the possible malfunction of the SR latch and increase the τ_{MC} , respectively. In [21, 22] SR latch is removed to avoid the problem presented in [2]. What's more, all the other problems, listed as: retiming MC scheme, modulus dependent divider delay, operation speed, external pulse generation circuit, and MC signal delay error, were also overcome in this two literatures. Nevertheless, the circuit complexity and power dissipation

was increased in it.

In this paper, we present an improved fractional-N pulse swallow frequency divider that resolves the problems mentioned above. A pulser was designed and inserted between DFF1 and B counter to reshape the DFF1's output signal, this design conquers the possible malfunction of the SR latch in the conventional structure. It also eliminates the problem of the wrong total division ratio. Besides, for improving the operating speed of the frequency divider we also proposed a retiming scheme of the MC.

The rest of the paper is organized as follows: Section 2 describes the conventional structures of the pulse swallow frequency divider. The proposed structure and building blocks of the pulse swallow frequency divider is presented in Section 3, results and discussion are described in Section 4. Finally, Section 5 presents the conclusions.

2. Conventional structures of pulse swallow frequency divider

For the sake of reducing the MC delay (τ_{MC}), a variety of pulse swallow frequency dividers have been proposed during the latest decades. While several problems advented accompany with these structures: the unwanted division ratio offset, the possible malfunction of the SR latch and the increased power consumption [1, 2, 3, 21, 22]. The conventional structure of the pulse swallow frequency divider is shown in Fig. 1(a) [1], its timing diagram is shown in Fig. 1(b). Since the prescaler is controlled by the MC signal, when $\text{MC} = 0$, the prescaler is divided by $P + 1$, and MC is controlled only by the B counter. However, MC signal's set and reset are triggered by different signals, namely Aout and Bout, as illustrated by the transition ① and ③ in Fig. 1(b). As a result, the division ratio for the first half period is $(B + 1) \times (P + 1)$ rather than $B \times (P + 1)$. Thus, the total division ratio is given by $PA + B + 1$, which causes an unwanted offset. It will complicate the interface logic between Σ - Δ modulator and the pulse swallow counter in the fractional-N PLL [2].

Another issue of the conventional structure is the possible malfunction of the SR latch. In order to avoid this problem, the falling edge of Aout must arrive later than Bout as illustrated by the transition ② in Fig. 1(b). If the falling edge of Aout arrives earlier than Bout as illustrated by the red transition ④ in Fig. 1(b), MC will be set via SR_Q, which leads to a wrong division ratio.

The other conventional structure of the pulse swallow frequency divider [2] is shown in Fig. 1(c). It adopts a single Bout to trigger the MC signal, as illustrated by the

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Fig. 1 (a) Conventional pulse swallow frequency divider. (b) Timing diagram of structure (a). (c) Conventional pulse swallow frequency divider with a delay element. (d) The timing diagram of structure (c).

transition ① in Fig. 1(d), which avoids the wrong division ratio. Besides, to generate a time interval τ_D , a delay element was employed, ensuring that the falling edge of the Aout arrives later than Bout, as illustrated by the transition ② in the Fig. 1(d). However, due to the immutable of the delay element, the time interval τ_D cannot vary with the input frequency [21, 22], which may cause the falling edge of the Aout arrives earlier than Bout. Therefore, the malfunction of SR latch may still appear in this structure.

3. The proposed structure and building blocks of the pulse swallow frequency divider

The proposed structure of pulse swallow frequency divider is shown in Fig. 2. This structure contains a 4/5 prescaler, a programmable counter (A), and a swallow counter (B). It adopts the synchronous setting function of the programmable counter and the swallow counter by a LOAD signal. While, the LOAD's falling edge arrives later than the PSO's rising edge, as shown by the transition ① in Fig. 3, which will leads to more than one counting of the B counter. To solve this problem, a pulser was designed and inserted between DFF1 and B counter to reshape the LOAD signal so as to generate a pulse signal. As shown by the red circle in the Fig. 3, the pulse signal's falling edge arrives earlier than PSO's rising edge.

In the traditional structure, the falling edge of Aout may arrive earlier than Bout, as shown in transition ② in Fig. 1(b) and transition ② in Fig. 1(d), causing an incorrect frequency division ratio of the divider. In the proposed structure, the pulse signal resets the Bout signal and generates a time interval Δt between the falling edge of the pulse signal and the Bout signal, as shown by the blue transition ②. It ensures that the falling edge of the pulse signal always arrives later than the Bout. Another design improvement of this structure is that the MC's set and reset are triggered by a single Bout signal, as shown by transition ③ and ④ in Fig. 3. As a result, the total division ratio is given by $PA + B$. Such a no-offset structure greatly simplifies the interface logic between Σ - Δ modulator and pulse swallow counter in the fractional-N PLL. The third improvement of this structure is that the new MC scheme was adopted by using a D flip-flop. As shown in

Fig. 2 Proposed pulse swallow frequency divider.

Fig. 3 The timing diagram of the proposed pulse swallow divider.

Fig. 3, the MC timing margin is extended and then the τ_{MC} is greatly reduced, which ensures that the operating speed of the divider is much improved. This feature is superior to the previous retiming structures [1, 2, 3, 21, 22].

3.1 Dual modulus prescaler

As is mentioned in the previous section, a divide-by-4/5 dual modulus prescaler was adopted. Its structure block diagram is shown in Fig. 4(a). It is a mixed-mode of synchronous logic and asynchronous logic [6, 27, 28]. When $MC = 0$, the synchronous logic cell divides the input signal by two, which then travels through the asynchronous divide-by-2 circuit, resulting in a total division ratio of 4. When $MC = 1$, once feedback is generated, the synchronous logic cell will be divided by three, and the total division ratio will be modulated to 5.

The divide-by-4/5 dual-modulus prescaler consists of three DFF, namely DFF0, DFF1, and DFF2. The implementation of these DFFs use true-single phase clock (TSPC) structure, which reduce the power consumption [4, 5, 6, 29, 30]. The DFFs outputs are defined as qb_0 , q_1 , and q_2 , and the divider state is defined as " $qb_0q_1q_2$ ", where the next state is calculated using: $qb_0^+ = qb_0$, $q_1^+ = qb_0$, and $q_2^+ = qb_2 * q_1 + q_2 * q_1$. In the case of $MC = 0$, DFF0's input d1 is set to high and behaves as a standard divide-by-2 DFF, as shown in Fig. 4(a). The output signal $PSO = q_2$, is just a reverse version of q_2 . There are four allowed states, as shown in Fig. 4(b), the shaded states represent states of $PSO = 1$. In the case of $MC = 1$, DFF0's input d1 is controlled by qb_1 and q_2 . When $qb_1 = 1$ and $q_2 = 1$, the DFF0's output retains high for two clock cycles. The

Fig. 4 (a) Block diagram of the divide-by-4/5 dual-modulus prescaler. State diagrams: (b) in the case of MC = 0 and (c) MC = 1.

Fig. 5 The schematic of the proposed swallow counter.

Fig. 6 The schematic of the pulser.

state diagram is illustrated in Fig. 4(c), where the division cycle repeats after five state transitions. The output signal $PSO = 1$ represents a 60% duty cycle of divide-by-5 clock. The divide-by-4/5 dual-modulus prescaler operates with an input clock frequency up to 7.04 GHz.

3.2 Pulser in swallow counter

The proposed swallow counter is shown in Fig. 5, which is composed of a pulser, a B counter, a SR latch, and a DFF. The pulser module is used to reshape the LOAD signal and to generate a narrow pulse signal to set the B counter. If the pulse width is too wide, the falling edge of the pulse signal will arrive later than the rising edge of PSO

Fig. 7 Chip micrograph of the fraction-N PLL with the proposed pulse swallow frequency divider.

signal, which causes a wrong frequency division ratio and results in a reduced operation speed of frequency divider. Therefore, the pulse width cannot be greater than the divide-by-4 period of PSO signal when the divider work at the highest frequency. On the other hand, if the pulse width is too narrow, it may cause the falling edge of the pulse signal arrives earlier than Bout signal, leading to SR latch malfunction. Thus, it is necessary to reduce the width of the pulse signal to an appropriate extent. In addition, for reducing the pulser response time, the output port of the pulser is inserted between the delay units D1 and D2, as is shown in Fig. 6. In this circuit the pulse signal only passes through the NAND and D1, which remarkably reduces the response time of pulser.

4. Results and discussion

The proposed modified pulse swallow frequency divider for a fractional-N PLL was fabricated in a 0.18 μm CMOS process. A chip micrograph of the proposed circuit is shown in Fig. 7. The fraction-N PLL with the proposed pulse swallow frequency divider circuit is used in a GNSS receiver. The active area of the PLL is 0.64 mm^2 while the pulse swallow frequency divider circuit is merely 0.054 mm^2 .

The simulation result of the proposed circuit is depicted in Fig. 8. Under the conditions of the process corners of fast and the temperature of 27°C, the frequency divider can be operated at a frequency of 7.04 GHz. Neither of the possible malfunction of the SR latch nor the unwanted division ratio are observed in the simulation. Fig. 9 shows the measured and simulated power consumption against input frequency at a division ratio of 59. The power consumption of the measurement and simulation results at minimal input frequency of 0.5 GHz are 0.72 mW and 0.51 mW, respectively. Generally, when the input frequency increases, the power consumption increases as well. While in the proposed structure, even the input frequency is up to 7.04 GHz, the power consumption of the measurement and simulation results are just 7.59 mW and 6.53 mW, respectively.

Table I presents the comparison of the proposed pulse swallow frequency divider with previously published results. The MC delay τ_{MC} of the proposed structure is as low as 120 ps, which is obviously better than the previous literatures. Therefore, the maximum input frequency $f_{in,max}$ can reach 7.04 GHz. Furthermore, benefit from the divider's circuits

Fig. 8 The simulation result of the pulse swallow frequency divider.

Fig. 9 Measured and simulated power consumption against input frequency.

Table I Performance comparison.

Reference	[1]	[2]	[3]	[22]	This work
Process Technology	0.4 μm	0.18 μm	0.13 μm	0.13 μm	0.18 μm
Div ratio	220–225	-	-	50–128	13–127
f_{inmax} (GHz)	5.2	6.6	1	5.4	7.04
t_{MC} (ps)	-	200	2000	-	120
Supply voltage (V)	2.6	1.8	0.7	1.2	1.8
Power (mW)	17	-	0.053	9	7.59

architecture and TSPC structure DFF, the power consumption is also lower than others. In summary, the proposed divider is very suitable for applications demand for high frequency and low power consumption.

5. Conclusion

A modified pulse swallow frequency divider for fractional-N frequency synthesizers was designed and implemented in a 0.18 μm CMOS process. A pulser was inserted between DFF1 and B counter, which solves the possible malfunction of SR latch and the problem of the wrong total division ratio in conventional structures. This method dramatically simplifies the circuit complexity as well as the interface

logic between Σ - Δ modulator and the pulse swallow counter. Meanwhile, the operating speed was greatly improved by the MC retiming scheme.

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