LETTER

Simulation study of an ultra-low specific on-resistance high-voltage pLDMOS with self-biased accumulation layer

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Abstract In this letter, a high-voltage p-channel Lateral Diffused Metal Oxide Semiconductor Transistor (pLDMOS) with self-biased accumulation layer is proposed. A poly-silicon layer is formed on the thin insulator layer, which locates at the surface of the P-drift region. During on-state, an automatically obtained negative voltage is applied on the poly-silicon to induce a hole accumulation layer at the surface of the P-drift region. Therefore, the specific on-resistance ($R_{on,sp}$) can be significantly reduced. Moreover, the permittivity of the gate insulator on the P-drift can be increased by selecting different insulator materials. Thus, the $R_{on,sp}$ can be further reduced due to more holes being accumulated at the surface of the P-drift. The simulation results shows that the $R_{on,sp}$ of the proposed pLDMOS can be dramatically reduced by 62.3% to 82.5% compared with that of the p-type Triple RESURF silicon limit. For the proposed pLDMOS, the transient Figure of Merit (FOM) is significantly improved by several to 10 times and the static Figure of Merit (FOM) is improved by several times compared with those of an Extended Gate pLDMOS (EG-pLDMOS) and a conventional pLDMOS.

Keywords: high-voltage pLDMOS, ultra-low specific on-resistance, accumulation layer, gate charge, Figure of Merit

Classification: Power devices and circuits

1. Introduction

High-voltage Lateral Diffused Metal Oxide Semiconductor Transistor (LDMOS) is very suitable for the applications of Smart Power Integrated Circuit [1, 2, 3, 4, 5, 6, 7, 8]. Usually, p-channel LDMOS (pLDMOS) is very attractive in the full complementary high-voltage driver ICs [9, 10, 11, 12, 13, 14]. However, due to low mobility of hole, the specific on-resistance ($R_{on,sp}$) is about 2–3 times larger than that of the n-channel LDMOS (nLDMOS). In order to reduce the $R_{on,sp}$, many solutions have been proposed [15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25], among which the Extended Gate pLDMOS (EG-pLDMOS) [15], applying hole accumulation layer to conduct current, can significantly reduce the $R_{on,sp}$. But the gate charge is dramatically increased due to that the extended gate covers the whole drift region. To significantly reduce the $R_{on,sp}$ without increasing its gate charges, a high-voltage pLDMOS with auto-accumulated hole layer in the P-drift region

during on-state is proposed and verified by the TCAD tool [27] in this letter.

2. Structure and mechanism of the proposed pLDMOS

Fig. 1. Structure of high-voltage pLDMOS. Insulator thickness $t_{ox} = 30$ nm. –HV represents negative high voltage.

a Extended Gate pLDMOS [15]

b Proposed pLDMOS with self-biased accumulation layer.

Fig. 1(b) shows the proposed pLDMOS. A thin layer insulator is formed on the surface of the P-drift region. Above the insulator, an N-type poly-silicon layer with OPTimized Variation Lateral Doping (OPT-VLD) [26] is implemented to improve the breakdown voltage. The poly-silicon has been proven to have an approximate breakdown voltage as that of the monocrystal silicon [28] or can be annealed by different techniques to approximate a monocrystal silicon [29]. Diode D_1 and D_2 are implemented in the poly-silicon near the drain and source region of the proposed pLDMOS, respectively. During the off-state, with the decreasing voltage of electrode D (to negative value), D_1 is forward biased and the anode of the diode D_0 (formed in the N-poly layer) is connected to electrode D through Floating Ohmic Contact-2 (FOC2) and D_1 . Therefore, D_0 is reverse biased to sustain the high voltage. Meanwhile, with the decreasing voltage of electrode D, the P-drift region with width of L_s as shown in Fig. 1(b) will be depleted. Then, the voltage of the Floating Ohmic Contact-1 (FOC1) will keep at a constant low value (negative value) [26], which means the voltage difference between electrode F and S (V_{FS}) keeps at a low negative

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value. The V_{FS} is stored in an external capacitor C_0 through diode D_2 as shown in Fig. 1(b). The EG-pLDMOS [15] is designed for comparison as shown in Fig. 1(a). A Conventional pLDMOS (C-pLDMOS) having the same structure as the EG-pLDMOS is also designed as comparison (no shown). The difference between the C-pLDMOS and the EG-pLDMOS is that the cathode N^+ of D_0 is connected to electrode S for the C-pLDMOS.

During the on-state, after the voltage of V_{DS} decreases to the on-state voltage drop (about 0 V), the V_{FS} is automatically applied on the N-poly layer and the reverse biased diode D_1 and D_2 help prevent the discharge of C_0 . Therefore, a hole accumulation layer is automatically formed at the surface of the P-drift layer without increasing the gate charges. By adjusting the L_s and the permittivity (value of K) of the insulator [30], the amount of accumulated holes can be adjusted to further reduce the $R_{on,sp}$. When the device is turned off again, the charges in the N-poly flows back to C_0 . Therefore, the charges are almost not consumed except for the leakage current flowing across D_1 and D_2 . The capacitance value of the external capacitor C_0 is selected to maintain a voltage of $0.9V_{FS}$ after part of the charges flows to the N-poly when the device is turned on. The calculated $C_0 = 9C_{ox}$, where C_{ox} is the capacitance of the Semiconductor/Insulator/Semiconductor (SIS) capacitor formed by the N-poly/Insulator/P-drift in the drift region (length: L_d).

3. Discussion of simulation results

Fig. 2. Influence of L_s on the auto-obtained power supply V_{FS} .

Fig. 2 shows the influence of L_s on the obtained low voltage V_{FS} . With the increase of L_s , the P-drift with width of L_s becomes fully depleted at a lower value of V_{DS} . Therefore, the voltage of V_{FS} is clamped at a lower value [26]. The V_{FS} is automatically applied on the N-poly to induce a hole accumulation layer on the surface of P-drift as shown in Fig. 3. With the increase of K , more holes are accumulated at the surface of the P-drift to conduct current. Therefore, with the increase of K and $|V_{FS}|$, the current capability of the proposed pLDMOS increases as shown in Fig. 4. The slopes of the I - V curves for the proposed one are much steeper than those of the C-pLDMOS and the EG-pLDMOS with the same K , which indicates the $R_{on,sp}$ of the proposed pLDMOS (extra length L_s is included when calculating $R_{on,sp}$) is dramatically reduced.

Fig. 3. Hole density distribution of proposed p-LDMOS along AA' in Fig. 1b with $V_{FS} \approx -12.5$ V.

Fig. 4. Comparison of output characteristics for different pLDMOSs with $V_{GS} = -5$ V. $K = 3.9$ (black color), 9.5 (red color), 20 (blue color).

Fig. 5. Comparison of $R_{on,sp}$ for different pLDMOS.

Fig. 5 reveals that the $R_{on,sp}$ of the proposed pLDMOS is reduced by 62.3% to 82.5% compared with that of the p-type Triple RESURF silicon limit. Moreover, by adjusting the K and V_{FS} , the $R_{on,sp}$ of the proposed pLDMOS can be reduced by 51% compared with that of the N-type Triple RESURF nLDMOS.

Fig. 6(a) and Fig. 6(b) demonstrates that the gate charge of the proposed pLDMOS is much smaller than that of the EG-pLDMOS. This is because the charges provided for the N-poly is stored in the capacitor C_0 rather than by the gate electrode. With the increase of K , the gate charges for the EG-pLDMOS increase more dramatically than those of the proposed one. This is because more charges are needed in the long N-poly layer for the EG-pLDMOS. For the proposed one, only a little more charges are needed to charge the increased gate capacitor (under G) due to larger K .

Fig. 6. Comparison of gate charges for different p-LDMOS. $V_{SF} \approx -5.5$ V (green color), -8.5 V (blue color), -12.5 V (red color). (a) Gate charges, (b) Enlarged view of the gate charges.

Table I. Comparison of transient FOM (FOM1) and static FOM (FOM2) for different pLDMOSs

Devices	--	FOM1 = $R_{on,sp} \bullet Q_G$ ($\Omega \bullet \text{nC}$)	FOM2 = $BV^2/R_{on,sp}$ (MW/cm^2)
Proposed with $V_{FS} \approx -12.5$ V	$K = 3.9$	4.0	5.00
	$K = 9.5$	6.6	7.63
	$K = 20$	9.9	10.77
Proposed with $V_{FS} \approx -8.5$ V	$K = 3.9$	4.4	4.51
	$K = 9.5$	7.5	6.67
	$K = 20$	11.8	9.22
Proposed with $V_{FS} \approx -5.5$ V	$K = 3.9$	4.9	4.02
	$K = 9.5$	8.9	5.66
	$K = 20$	14.1	7.69
EG-pLDMOS	$K = 3.9$	47.9	4.08
	$K = 9.5$	83.8	5.69
	$K = 20$	121.0	7.69
C-pLDMOS	$K = 3.9$	10.7	1.86

Table I clearly shows that the transient Figure of Merit (FOM1) of the proposed one is over ten times improved (smaller value) compared with that of the EG-pLDMOS under the same K . Besides, the static Figure of Merit (FOM2) with $V_{FS} \approx -12.5$ V and -8.5 V are also improved (larger value) compared with those of the EG-pLDMOS. Both the FOM1 and FOM2 of the proposed one are improved by several times compared with those of the C-pLDMOS.

Fig. 7(a)–Fig. 7(d) shows that the turning-on time of the C-pLDMOS, EG-pLDMOS and the proposed one are almost the same. However, the turning-off time (t_f) of the EG-pLDMOS is larger than that of the proposed pLDMOS under the same K , as shown in Fig. 7(a)–Fig. 7(d), due to

Fig. 7. Comparison of transient characteristics for different p-LDMOSs. Test condition $-HV = -300$ V with resistive load connected to D. (a) Between the C-pLDMOS and EG-pLDMOS, (b) Between the C-pLDMOS and proposed pLDMOS with $V_{SF} \approx -5.5$ V, (c) Between the C-pLDMOS and proposed pLDMOS with $V_{SF} \approx -8.5$ V, (d) Between the C-pLDMOS and proposed pLDMOS with $V_{SF} \approx -12.5$ V.

that the gate voltage decreasing ratio of the EG-pLDMOS is slowed down by the large capacitor formed by the N-poly/Insulator/P-drift. The t_f of the proposed pLDMOS is a little larger than that of the C-pLDMOS due to that the accumulated holes in the P-drift needs to be extracted out. With the increase of K , more time is needed, as shown in Fig. 7(b), Fig. 7(c) and Fig. 7(d), due to more holes are accumulated.

4. Conclusion

A high-voltage pLDMOS with self-biased accumulation layer is proposed to significantly reduce the specific on-resistance and the gate charges. The simulation results demonstrate that both the transient and static Figure of Merit are significantly improved compared with those of the C-pLDMOS and EG-pLDMOS.

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