LETTER

An IAOT controlled current-mode buck converter with RC-based inductor current sensor

Chanrong Jiang¹, Changchun Chai¹, Yi Yang¹, Yuqian Liu^{1a}, and Yintang Yang¹

Abstract An improved adaptive-on-time (IAOT) controlled current mode buck converter with RC-based current-sensing circuit and internal soft-start property is presented in this paper. First, the inductor current is sensed by a resistor-capacitor (RC) network, which can fully sense the trend of inductor current with high accuracy. Second, an IAOT control circuit is used to realize the on-time of the power switch adaptively changing with the operation conditions. In addition, the overshoot (undershoot) voltages are reduced by making T_{ON} adaptively shorter (longer) during the unloading (loading) transient due to the IAOT control. Third, soft start operation protects the circuit from large in-rush current during startup of the converter. Fourth, the proposed buck converter was implemented with standard 0.18- μm CMOS process. Simulation outcomes have shown an input voltage of 5 V, when the output voltage is ranging from 1.2 V to 3.6 V, with a maximum conversion efficiency of 98% (heavy loads) and 94% (light loads), making the buck converter quite useful in power management ICs.

Keywords: buck converter, inductor current sensor, improved adaptive on time (IAOT), soft-start, transient response

Classification: Integrated circuits

1. Introduction

With the rapid development of portable electronic devices, the requirements for power management systems are getting higher and higher. How to reduce the design complexity, reduce the cost, improve the conversion efficiency and speed up the transient response of the power supply system are the most basic and significant issues now [1, 2, 3, 4, 5]. As one of the power sources, DC-DC switching power supply is widely used in the modern electronic product market due to its high integration, high efficiency, small size and strong anti-interference ability [6, 7]. The voltage mode control has simple structure and mechanism, which is easy to model for analysis and simulation. However, the delay of the output inductor and capacitor makes the system has a slow transient response to the input voltage variation, and the output LC filter introduces double poles to the control loop, increasing the design difficulty of the compensation network. The current mode control method introduces a current detection module based on the voltage mode, which has a faster transient response. However, there are a lot of difficulties and problems on circuit

realization of the current-sensing function, especially in accurate current sensing [8, 9, 10].

Many methods have been proposed and developed for current-sensing, such as connecting a series resistor with the inductor, detecting the on-resistance of the power MOSFET [11] and the equivalent series impedance of the power inductor [12]. A separate sense FET can also be used as an on-chip current sensor [13]. The main problem of series resistor is the high power dissipation. While the main concern of the on-resistance of the power MOSFET or the equivalent series impedance of the inductor is the uncontrollability. Among them, the on-chip current sensor with a sense FET is the most popular technique for integrated current-mode buck converter due to its relatively high accuracy and simple circuit structure [14]. However, there are still problems with efficiency and circuit complexity in IC design. In addition, poor current detection accuracy is also another key issue [15].

The simplest way of inductor current sensing is to use a resistor-capacitor (RC) network across the inductor which does not require any feedback network [16], widely used in the hysteretic buck converter. However, they suffered from not only electromagnetic interference (EMI) problem due to the switching frequency to be continuously changing, but also a large output ripple voltage due to the wide hysteresis window range. What's more, the output voltage has nonzero dc-offset from the desired level. To overcome these limitations, several hysteretic converters have been reported that provide fixed switching frequency and accurate dc level of the output [16, 17, 18]. However, they suffer from noise due to the differentiator for amplifying ripple voltage [17], or generate high switching loss in the converter [18].

In summary, there are four main issues to be resolved in designing a current mode buck converter, that is, simple and accurate inductor current sensing circuit, error of the output voltage caused by the series resistance of the inductor, varying switching frequency due to the operating condition and transient response.

An improved adaptive on time (IAOT) controlled current mode buck converter presented in this paper addresses the above problems. First, the inductor current information is obtained through a low-pass filter composed by an RC network. Second, in order to remove the dc-offset of the output voltage, an additional error amplifier (EA)-based feedback path with compensation network is employed. Third, the switching frequency is regulated by an IAOT controller. Fourth, the output of the amplifier, V_c , is

¹Wide Bandgap Semiconductor Technology Disciplines State Key Laboratory, Xidian University, Xi'an 710071, P.R. China
a) yuqianliuxd@163.com

DOI: 10.1587/ele.17.20190757
Received December 30, 2019
Accepted January 17, 2020
Publicized January 31, 2020
Copyrighted February 25, 2020

used as the voltage control signal of the adaptive on-timer, which can reduce the overshoot by making T_{ON} adaptively shorter during the unloading transient and vice versa. In addition to solving the above problems, a simple and efficient on-chip soft-start circuit is also implemented to suppress the inrush current and overshoot voltage so that the over-current and over-voltage damages are avoided and efficiency is not hampered even during the power-on phase of the buck converter.

Rest of the paper is organized as follows: Section 2 describes the architecture and implementation of the proposed buck converter. Section 3 presents the operation modes and circuit implementation of various blocks including a novel on-chip soft-start circuit. The simulation results and discussion are given in Section 4, which is followed by conclusions in Section 5.

2. Architecture and control strategy

Fig. 1 shows the block diagram of the proposed IAOT controlled current-mode buck converter with an RC current-sensor and soft-start circuit. When the system is powered up, the converter moves into soft-start mode until the output voltage reaches the rated level. The converter consists of two control loops. The first loop is a voltage feedback loop for the accurate level of the output voltage while the second loop is an improved current-controlled loop, which increase the bandwidth of the converter's closed-loop gain to improve the transient response and increase the efficiency of the converter [19]. As the complementary power transistors M_1 and M_2 turns on and off, switching node V_{sw} oscillates in the form of a pulse wave between voltage levels of approximately V_{in} and GND. This square pulse is integrated by the RC passive filter and acts as the ramp signal for the comparator. Since the duration of the high level of V_{sw} changes with the duty ratio, the common mode level of the low-pass filtered signal V_a will also change with the duty cycle. Therefore, the converter can achieve a wide duty cycle range without an external ramp signal. What's more, the introduction of the IAOT circuit enables the converter to achieve a constant switching frequency under continuous conduction mode (CCM) while the zero current detection (ZCD) circuit ensures the switching frequency under discontinuous conduction mode (DCM) proportional to the load current. By the cooperation of these two circuits, the ability to resist EMI and the conversion efficiency under DCM can be

Fig. 1. Proposed IAOT controlled buck converter.

further improved. In order to accelerate the transient response speed, the output of the EA is used as the voltage control signal of the IAOT, which reduces the overshoot by making T_{ON} adaptively shorter (longer) during the unloading (loading) transient.

3. Operating mode and circuit implementation

3.1 Continuous conduction mode

In order to achieve a constant switching frequency under CCM, an improved adaptive on-time (IAOT) control circuit is introduced in the converter, as shown in Fig. 2. The increase amount of the inductor current during the ON state is given by:

$$\Delta I_L(+) = \frac{(V_{in} - V_{DSP} - I_L \times R_L) - V_O}{L} \times T_{ON} \quad (1)$$

The decrease amount of the inductor current during the OFF state is given by:

$$\Delta I_L(-) = \frac{V_O + (V_{DSN} + I_L \times R_L)}{L} \times T_{OFF} \quad (2)$$

Where V_{DSP} and V_{DSN} represent the on-state voltage drop of the two power transistors, respectively. R_L is the equivalent series resistance of the inductor. In steady state conditions, there is no net increase or decrease in inductor current from cycle to cycle. Therefore, these two equations should be equated and solved for the switching frequency f_s under CCM. It is worth noticing that in order to simplify the calculation, the influence of V_{DSP} , V_{DSN} and R_L was ignored.

$$f_s = \frac{V_O}{V_{in}} \times \frac{1}{T_{ON}} \quad (3)$$

From Eq. (3), T_{ON} can be adjusted to make the switching frequency constant without being affected by the input and output voltages. Based on the traditional COT control, an input voltage feedforward control loop and an output voltage feedback loop are introduced in Fig. 2. The expression of T_{ON} is obtained as follows:

$$T_{ON} = \frac{C_1 \times V_O}{g \times V_{in}} \quad (4)$$

Where g is the scale factor of the voltage-controlled current source (VCCS). Upon substituting Eq. (4) into Eq. (3), the final expression of f_s can be obtained as follows:

$$f_s = \frac{V_O}{V_{in}} \times \frac{g \times V_{in}}{C_1 \times V_O} = \frac{g}{C_1} \quad (5)$$

Fig. 2. The improved adaptive on-time controller.

From Eq. (5), while ignoring the non-ideal effects, the IAOT circuit can achieve a constant switching frequency under CCM.

It is well known that the output impedance of the converter has reasonable peak due to the LC resonance of the filter circuit. This resonance causes a large overshoot and undershoot voltages on the output for the load changes [20]. For a COT controlled buck converter, when the load current steps down during the on-time of the power transistor, the controller cannot terminate the conduction of the control switch until T_{ON} expires, which increases the overshoot of the output voltage. As will be explained below, during the normal working process, the average voltage of V_a is similar to the output voltage, and the value of V_c is consistent with V_a due to the clamping effect of the comparator. Compared with V_o , V_a and V_c can quickly sense the step change of the load current, so using V_c instead of V_o as the voltage control signal of the IAOT circuit can further improve the transient response of the buck converter.

3.2 Discontinuous conduction mode

In addition to T_{ON} and T_{OFF} similar to CCM, there is also an idle state under DCM. Their proportions in the switching cycle are $D1$, $D2$ and $D3$, respectively. The increase of the inductor current during the ON state is given by:

$$\Delta I_L(+) = \frac{V_{in} - V_o}{L} \times T_{ON} = \frac{V_{in} - V_o}{L} \times D_1 \times T_s = I_{pk} \quad (6)$$

Because the current starts at zero in DCM, so the ripple current, $\Delta I_L(+)$, is also the peak inductor current, I_{pk} . Similar, the decrease of the inductor current during the OFF state is given by:

$$\Delta I_L(-) = \frac{V_o}{L} \times T_{OFF} = \frac{V_o}{L} \times D_2 \times T_s \quad (7)$$

As in the CCM case, the current increase during the ON state is equal to the current decrease during the OFF time. Eq. (7) and Eq. (8) can be equated and solved for V_o .

$$V_o = V_{in} \times \frac{D_1}{D_1 + D_2} \quad (8)$$

The output current is the average ss of the inductor current, which can be obtained from Fig. 3.

$$I_o = I_{L(avg)} = \frac{I_{pk}}{2} \times \frac{D_1 \times T_s + D_2 \times T_s}{T_s} = \frac{V_o}{R} \quad (9)$$

Where R is the load resistance. From Eq. (8) and Eq. (9), we can obtain the expression of the switching period T_s .

$$T_s = \frac{T_{ON}^2 \times V_{in} \times (V_{in} - V_o) \times R}{2 \times V_o^2 \times L} \quad (10)$$

Fig. 3. Waveforms of discontinuous conduction mode.

For a given V_{in} and V_o , T_{ON} is constant due to the presence of the IAOT controller. So T_s will increase with R and the value of L will also affect it. Too large L will not only increase the area but also increase the switching frequency, which will increase the power loss caused by frequent switching operations. Too small L will make the switching frequency too low, which will reduce the conversion efficiency. This leaves L as one of the significant parameters to maintain a reasonable switching frequency under DCM.

3.3 Passive-current-sensing circuit

A simplified schematic of the power stage is shown in Fig. 4. The RC switching loop was firstly analyzed without the effects of the inductance, output capacitance and the load resistance. The two power transistors turn on and off in a complementary mode. When M_1 turns on, the capacitor C is charged by the difference of the input voltage and the voltage through the resistor, R [21]. And when M_2 turns on, C is discharged through R and M_2 . The expression of V_a , the output of the RC circuit, is obtained as follows:

$$V_a = \frac{V_{sw}}{1 + sRC} \quad (11)$$

When M_1 turns on and M_2 turns off, there is

$$V_a(+) = \frac{V_{sw}(+)}{1 + sRC} = \frac{V_{in} - I_L(+) \times R_{ON1}}{1 + sRC} \quad (12)$$

When M_1 turns off and M_2 turns on, there is

$$V_a(-) = \frac{V_{sw}(-)}{1 + sRC} = \frac{-I_L(-) \times R_{ON2}}{1 + sRC} \quad (13)$$

Among them, V_{sw} represents the voltage of the common mode of M_1 and M_2 , R_{ON1} and R_{ON2} represent the turn-on voltage drop across M_1 and M_2 , respectively. From Eq. (12) and (13), it can be seen that during the whole switching cycle, the variation of V_a can well reflect the variation of I_L . Ideally, at steady state, the average current flowing through the capacitor C is zero. Therefore, the introduction of the RC network in the power stage not only collect the inductor current information throughout the cycle, but also does not generate additional consumption.

3.4 Soft-start circuit

During the startup phase of the DC-DC switching power supply, the output cannot be established instantaneously due to the loop response, causing the loop to operate at 100% duty cycle [22, 23, 24]. At this time, both the output voltage and the inductor current will cause an overshoot, damaging the components of the converter and other electronic equipment in the circuit [25, 26].

Fig. 4. Power stage of the buck converter with RC network.

An on-chip soft-start circuit composed of a ramp signal generation circuit and a gating circuit of high side transistor is used in this paper to overcome the above problem. Firstly, the ramp signal control the positive input of the amplifier to rise slowly from zero and switches to the control of V_{REF} . At the same time, by adjusting the conduction size of the high-side power transistor M_1 , the peak values of the inductor current and the output voltage are further limited.

As shown in Fig. 1, the designed aspect ratios of power transistors M_{P0} , M_{P1} , M_{P2} and M_{P3} are successively increased, producing a reducing on-resistance. Thereby, the peak value of the inductor current is greatly limited. In order to reduce unnecessary energy losses, all transistors are turned on within 120 μ s, and the system continues to complete the soft-start process in the specified soft-start time. The gating circuit of high-side transistor works in the early stage of soft-start, and doesn't have any influence on the whole circuit under the steady state.

3.5 Ramp signal generating circuit

The principle of the ramp signal generation is to charge a capacitor with a current source. The slope can be controlled by changing the charging current or the value of the capacitor. Considering the requirements of the low power consumption, the charging current should not be too large while a large capacitor will occupy a large chip area. With regards to this, a capacitance multiplication circuit is used in this paper. As shown in Fig. 5, the value of C_2 is greatly reduced by reasonably selecting the aspect ratio of M_{12} and M_{13} , thereby greatly reducing the chip area. The circuit starts its soft-start operation the time EN turns to high level. Firstly, capacitor C_2 is charged by current source I_1 while a ramp voltage signal is generated across the capacitor. The ramp signal is then compared to V_{REF} after passing through a voltage buffer. Before V_s rises to V_{REF} , the reference selection circuit selects V_s to be the reference signal of EA. When V_s is greater than V_{REF} , I_2 also charges the capacitor C_2 . Then V_s rises rapidly to get the system out of the soft start state.

Fig. 5. Ramp signal generating circuit.

4. Results and discussion

First, to verify the accuracy of the RC network for sampling the information of the inductor current, waveforms of V_a , the output of the RC network, and the inductor current are shown in Fig. 6. The variation trend of V_a is proportional to I_L without any phase delay, proving that the feedback of V_a into the control loop can effectively improve the transient response performance.

Fig. 6. Waveforms of the inductor current and V_a .

Then, system level simulation results are shown in Fig. 7. It can be seen that the inductor current rises step by step with the amplitude of each rise 100 mV while V_o also ramps up slowly. According to the simulation results, soft-starting ensures the inductor current and output voltage rising slowly without large overshoot, eliminating the chances of damaging the external power element due to large in-rush current.

Fig. 7. System level simulation results.

The IAOT control method is proposed to achieve fast-transient response and produce a fixed switching frequency under CCM. Fig. 8 illustrates the operation waveforms of the output voltage and inductor current during load transient period. When load current increases, V_o decreases as charge is supplied from the output capacitor. For the load current steps up from 80 mA to 240 mA, the output recovers its desired level with the error smaller than 1% in 5 μ s and the undershoot voltage is only 3 mV. Due to the introduction of the EA, the dc-offset of the output voltage is controlled within 1 mV, 0.08% of the desired value. The variation in output voltage due to load changes is almost zero, proving that the converter has good load regulation performance.

Fig. 8. Transient response waveforms for step up transient.

Conventional COT control uses large R_{ESR} to get the sensing signal in phase with the inductor current [27]. When step-up load current occurs, COT control extends the switching frequency due to the insertion of minimum off-time to rapidly recover V_o . In contrast, in the IAOT control, using V_c instead of V_o as the control voltage can respond quickly according to the changes in load. Fig. 9(a)

shows the transient response without the minimum off-time period. On the other hand, when step-down load current occurs, as shown in Fig. 9(b), the IAOT control extends the off-time period or even removes the minimum off-time to extend the duty cycle to 100% until V_o is pulled low to the desired value, which not only further enhance the transient response, but also overcomes the disadvantage of redundant on-time in the additional current feedback path (ACFP) control [27]. It can be seen from the simulation results that both the elimination of the inverse inductor current and the extension of the duty cycle can accelerate the overall transient response.

Fig. 9. Transient response waveforms when load current changes from (a) light to heavy (b) heavy to light.

The simulated switching periods, shown in Fig. 10, proves that the proposed IAOT control circuit enabled the proposed buck converter in CCM to fix the switching frequency of 1 MHz. When the output voltage ranges from 1.2 to 3.6 V, the variation is less than 3.5%, as shown in Fig. 10(a). It is worth noticing that compared to COT control, the converter under IAOT control not only achieve a quasi-constant switching frequency, but also a larger output voltage range can be got without additional slope compensation. When the load current changes from 300 mA to 1 A, its switching frequency variation is less than 1.8%, as shown in Fig. 10(b). Both of the IAOT control and COT control have little change with the load current, which indicates that on the basis of inheriting the advantages of the simple structure of COT, IAOT further stabilize the switching frequency under different output voltages.

Fig. 10. Switching frequency with (a) output voltage (b) load current.

The power efficiency is simulated versus the load current and the output voltage as shown in Fig. 11. With a 5 V input voltage, the maximum efficiency of the converter is 98% at 240 mA load current and 3.6 V output voltage. The maximum efficiency in low-frequency mode is 94% at 36 mA load current and the output voltage is

3.6 V. The performance comparison with previous buck converters is summarized in Table I. And the results show that this paper has the best value of FoM, meaning the fastest recovery of the output during the load transient. The figure of merit (FOM) in Table I is the reciprocal of the FOM of [28].

Fig. 11. Conversion efficiency versus load current and output voltage.

Table I. Summary and comparison

Reference	[2] (w/o PLL)	[29]	[30]	This work
Results	Simulation	Simulation	Measured	Simulation
Technology	0.35 μm	16 nm	0.35 μm	0.18 μm
Control	CAOT ¹	PWM	HVC ²	IAOT
Input voltage	2.6–4.0 V	2.3–3.6 V	2.4–4.2 V	5 V
Output voltage	1–2 V	0.8 V	1.8 V	1.2–3.6 V
Inductor	4.7 μH	4.7 μH	4.7 μH	4.7 μH
DCR	100 m Ω	200 m Ω	N/A	50 mΩ
Capacitor	10 μF	10 μF	4.7 μF	20 μF
Switching frequency	1 MHz	0.5 and 1 MHz	1 MHz	1 MHz
Maximum load current	0.6 A	0.4 A	0.5 A	1 A
Peak efficiency	95.05%	95.25%	95%	98%
FoM	3.42	0.63	1.9	3.56

¹CAOT: Current-Mode Adaptive on-Time Control;

²HVC: Hysteretic Voltage Control

$$FOM = \frac{\text{Peak Efficiency (\%)} \times \text{Load Current Step (A)} \times \text{Max. Load Current (A)}}{\text{Recovery Times (\mu s)}}$$

5. Conclusion

To realize a buck converter with high accuracy of output regulation and fast transient response, the IAOT controlled method was implemented and the inductor current was sensed by an RC network. The switching frequency was regulated by the IAOT circuit to be constant regardless of the operating condition under CCM. While in DCM, considering the conversion efficiency, the switching frequency of the converter is proportional to the load current. Moreover, the transient response is also improved due to the improvement of the IAOT structure. The proposed buck converter implemented in a 0.18 μm CMOS technology provided the output voltage ranging from 1.2 V to 3.6 V with a 5 V input voltage. The maximum power conversion

efficiency is 98% for a 5 V input voltage and 3.6 V output voltage, letting the proposed buck converter be well suited for high-performance portable devices.

Acknowledgments

Projected supported by the National Nature Science Foundation of China (No. 61974116).

References

- [1] Y.-T. Chen, *et al.*: “A DC-DC buck converter chip with integrated PWM/PFM hybrid-mode control circuit,” International Conference on Power Electronics & Drive Systems IEEE (2010) (DOI: [10.1109/PEDS.2009.5385699](https://doi.org/10.1109/PEDS.2009.5385699)).
- [2] J.-J. Chen, *et al.*: “A new fast-response current-mode buck converter with improved I^2 -controlled techniques,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **26** (2018) 903 (DOI: [10.1109/TVLSI.2018.2796088](https://doi.org/10.1109/TVLSI.2018.2796088)).
- [3] Y.-Z. Ma, *et al.*: “A current mode buck/boost DC-DC converter with automatic mode transition and light load efficiency enhancement,” IEICE Trans. Electron. **E98.C** (2015) 496 (DOI: [10.1587/transele.E98.C.496](https://doi.org/10.1587/transele.E98.C.496)).
- [4] Y. Ma, *et al.*: “A high efficiency hybrid step-up/step-down DC-DC converter using digital dither for smooth transition,” IEICE Trans. Fundamentals **E94-A** (2011) 2685 (DOI: [10.1587/transfun.E94.A.2685](https://doi.org/10.1587/transfun.E94.A.2685)).
- [5] M. Z. Malik, *et al.*: “A new modified quadratic boost converter with high voltage gain,” IEICE Electron. Express **14** (2017) 20161176 (DOI: [10.1587/eleex.13.20161176](https://doi.org/10.1587/eleex.13.20161176)).
- [6] H. Nam, *et al.*: “A buck converter with adaptive on-time PFM control and adjustable output voltage,” Analog Integr. Circuits Signal Process. **71** (2012) 327 (DOI: [10.1007/s10470-011-9802-7](https://doi.org/10.1007/s10470-011-9802-7)).
- [7] D.-H. Jung, *et al.*: “0.293-mm² fast transient response hysteretic quasi- V^2 DC-DC converter with area efficient time-domain-based controller in 0.35- μ m CMOS,” IEEE J. Solid-State Circuits **53** (2018) 1844 (DOI: [10.1109/JSSC.2018.2805884](https://doi.org/10.1109/JSSC.2018.2805884)).
- [8] C. F. Lee, *et al.*: “A monolithic current-mode CMOS DC-DC converter with on-chip current-sensing technique,” IEEE J. Solid-State Circuits **39** (2004) 3 (DOI: [10.1109/JSSC.2003.820870](https://doi.org/10.1109/JSSC.2003.820870)).
- [9] C.-H. Chang and R. C. Chang: “A novel current sensing circuit for a current-mode control CMOS DC-DC buck converter,” IEEE VLSI-TSA International Symposium on VLSI Design, Automation and Test (2005) (DOI: [10.1109/vdat.2005.1500034](https://doi.org/10.1109/vdat.2005.1500034)).
- [10] J.-J. Chen, *et al.*: “An active current-sensing constant-frequency HCC buck converter using phase-frequency-locked techniques,” IEEE Trans. Ultrason., Ferroelectr., Freq. Control **55** (2008) 761 (DOI: [10.1109/TUFFC.2008.710](https://doi.org/10.1109/TUFFC.2008.710)).
- [11] T. A. Smith, *et al.*: “Controlling a DC-DC converter by using the power MOSFET as a voltage controlled resistor,” IEEE Trans. Circuits Syst. I, Fundam. Theory Appl. **47** (2000) 357 (DOI: [10.1109/81.841918](https://doi.org/10.1109/81.841918)).
- [12] H. P. Forghani-zadeh, *et al.*: “An accurate, continuous, and lossless self-learning CMOS current-sensing scheme for inductor-based DC-DC converters,” IEEE J. Solid-State Circuits **42** (2007) 665 (DOI: [10.1109/JSSC.2006.891721](https://doi.org/10.1109/JSSC.2006.891721)).
- [13] H. Y. H. Lam, *et al.*: “Loop gain analysis and development of high-speed high-accuracy current sensors for switching converters,” IEEE International Symposium on Circuits and Systems (2004) (DOI: [10.1109/ISCAS.2004.1329936](https://doi.org/10.1109/ISCAS.2004.1329936)).
- [14] J.-W. Ha, *et al.*: “A fast response integrated current-sensing circuit for peak-current-mode buck regulator,” J. Semicond. Technol. Sci. **14** (2014) 810 (DOI: [10.5573/JSTS.2014.14.6.810](https://doi.org/10.5573/JSTS.2014.14.6.810)).
- [15] P. Midya, *et al.*: “Sensorless current mode control—An observer-based technique for DC-DC converters,” IEEE Trans. Power Electron. **16** (2001) 522 (DOI: [10.1109/63.931070](https://doi.org/10.1109/63.931070)).
- [16] M.-G. Jeong, *et al.*: “A current-mode hysteretic buck converter with multiple-reset RC-based inductor current sensor,” IEEE Trans. Ind. Electron. **66** (2019) 8445 (DOI: [10.1109/TIE.2018.2889613](https://doi.org/10.1109/TIE.2018.2889613)).
- [17] Y. Zheng, *et al.*: “A fast-response pseudo-PWM buck converter with PLL-based hysteresis control,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **20** (2012) 1167 (DOI: [10.1109/TVLSI.2011.2156437](https://doi.org/10.1109/TVLSI.2011.2156437)).
- [18] M. K. Song, *et al.*: “A 6 A 40 MHz four-phase ZDS hysteretic DC-DC converter with 118 mV droop and 230 ns response time for a 5 A/5 ns load transient,” IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC) (2014) (DOI: [10.1109/isscc.2014.6757346](https://doi.org/10.1109/isscc.2014.6757346)).
- [19] Y. Y. Yan, *et al.*: “I₂ average current mode control for switching converters,” 2013 IEEE Applied Power Electronics Conference and Exposition (APEC) (2013) (DOI: [10.1109/APEC.2013.6520214](https://doi.org/10.1109/APEC.2013.6520214)).
- [20] T. Nabeshima, *et al.*: “Analysis and design considerations of a buck converter with a hysteretic PWM controller,” Proc of Power Electronics Specialists Conference (2014) 1711 (DOI: [10.1109/PESC.2004.1355684](https://doi.org/10.1109/PESC.2004.1355684)).
- [21] X. W. Zhou, *et al.*: “A novel current-sharing control technique for low-voltage high-current voltage regulator module applications,” IEEE Trans. Power Electron. **15** (2000) 1153 (DOI: [10.1109/63.892830](https://doi.org/10.1109/63.892830)).
- [22] M. Al-Shyoukh, *et al.*: “A compact ramp-based soft-start circuit for voltage regulators,” IEEE Trans. Circuits Syst. II, Exp. Briefs **56** (2009) 535 (DOI: [10.1109/tcsii.2009.2022205](https://doi.org/10.1109/tcsii.2009.2022205)).
- [23] Y.-M. Li, *et al.*: “A digital-controlled soft-start circuit for negative output DC-DC converter,” J. Circuits Syst. Comput. **28** (2019) 1950067 (DOI: [10.1142/s0218126619500671](https://doi.org/10.1142/s0218126619500671)).
- [24] P.-J. Liu, *et al.*: “A current-mode buck converter with a pulse-skipping soft-start circuit,” 2013 IEEE 10th International Conference on Power Electronics and Drive Systems (PEDS) (2013) (DOI: [10.1109/PEDS.2013.6527025](https://doi.org/10.1109/PEDS.2013.6527025)).
- [25] B. Yuan, *et al.*: “Ramp-based soft-start circuit with soft-recovery for DC-DC buck converters,” Electron Devices and Solid-State Circuits (EDSSC) (2013) (DOI: [10.1109/EDSSC.2013.6628196](https://doi.org/10.1109/EDSSC.2013.6628196)).
- [26] L. Huang, *et al.*: “A high speed on-chip soft-start technique with high start-up stability for current-mode DC-DC converter,” IEEE Access **7** (2019) 27579 (DOI: [10.1109/ACCESS.2019.2901529](https://doi.org/10.1109/ACCESS.2019.2901529)).
- [27] W.-H. Yang, *et al.*: “A constant-on-time control DC-DC buck converter with the pseudo wave tracking technique for regulation accuracy and load transient enhancement,” IEEE Trans. Power Electron. **33** (2018) 6187 (DOI: [10.1109/TPEL.2017.2746659](https://doi.org/10.1109/TPEL.2017.2746659)).
- [28] Y. S. Hwang, *et al.*: “A fast transient response flying-capacitor buck-boost converter utilizing pseudocurrent dynamic acceleration techniques,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **23** (2015) 1155 (DOI: [10.1109/TVLSI.2014.2323313](https://doi.org/10.1109/TVLSI.2014.2323313)).
- [29] A. Rehani, *et al.*: “A high-efficient current-mode PWM DC-DC buck converter using dynamic frequency scaling,” IEEE Computer Society Annual Symposium on VLSI (ISVLSI) (2018) (DOI: [10.1109/isvlsi.201800090](https://doi.org/10.1109/isvlsi.201800090)).
- [30] C.-S. Huang, *et al.*: “A fast-transient quasi- V^2 switching buck regulator using AOT control,” IEEE Asian Solid-State Circuits Conference (2011) 53 (DOI: [10.1109/asscc.2011.6123597](https://doi.org/10.1109/asscc.2011.6123597)).