Investigation of soft ESD failure on capacitive transimpedance amplifier for hybrid integrated infrared sensor

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**Abstract** In this letter, an experiment is designed to validate the soft ESD failure. The capacitive transimpedance amplifier (CTIA) circuit used in the hybrid integrated infrared sensor is chosen as the prototype for its characteristic of ESD-protection-device-free. The experiments show that under the ESD event with the rising pulse voltage, the induced leakage current in the CTIA circuit increases as well. As the pulse voltage exceeds a certain threshold point, the CTIA circuit fails to work anymore. The EMMI measurement helps to demonstrate the existence and location of the leakage path.

**Keywords:** soft ESD failure, infrared sensor, CTIA

**Classification:** Integrated circuits

1. Introduction

For its catastrophic consequence, electrostatic discharge (ESD) induced hard failures such as thermal breakdowns of microelectronic device and metal interconnect, have been well understood and drawn much attention of the researchers in the world \([1, 2, 3, 4, 5, 6, 7, 8]\). Nevertheless, the problems of ESD induced soft failure such as performance degradation and increased leakage current, are not still fully comprehended and investigated \([9, 10, 11, 12]\). This problem might raise great concerns in some specific application fields, especially for the hybrid integrated infrared sensor system with high sensitivity. For the infrared sensor, infrared radiation from the target is transferred into opto-current by the detector, then converted into the amplified voltage by the readout circuit. Traditionally, the infrared detector and readout circuit are fabricated with different materials and processes. After that, indium bump is used to interconnect both chips \([13, 14, 15, 16]\). Generally speaking, for the infrared sensor with high sensitivity, the current generated by the detector is as weak as tens of pA. Any potential leakage current will compromise the performance. And in order to improve the resolution of the infrared image, a large number of detector pixels as many as millions are often placed in a very compact array. With the state of art fabrication process, the pixel pitch has been scaled to tens of µm. Therefore, for the reason of weak current sensing capability and small pixel area, no ESD protection devices are included in the readout circuit. In such circumstance, the unavoidable ESD event that happens in the process of dicing, assembly and package, might do harm to the unprotected readout circuit. Therefore, to illustrate the potential soft failure problem in infrared readout circuit, the functionalities of a capacitive transimpedance amplifier (CTIA), which is often adopted as the frontend readout circuit \([17, 18, 19, 20]\), are investigated before and after ESD event.

2. Basic operation of CTIA circuit

CTIA has been long chosen as the fronted readout circuit to convert the opto-current into voltage for its superior noise and area performance. Fig. 1 depicts the simplified circuit. Two phase operation of CTIA works as follow: in the reset phase, the switch S1 is closed, the amplifier in the CTIA is connected as unit gain configuration to set an initial output voltage; in the integration phase, S1 is opened, the sink/source current from the detector is integrated across the feedback capacitor C\(_i\). The developed output voltage is linearly changed with the passing integration time, and the final voltage is sampled by the later stage at the end of the integration phase \([21, 22]\). To accommodate the large dynamic range of the opto-current, optional feedback capacitors with different values are often designed. The area occupied by the CTIA pixel should match with that of the detector pixel. In principle, any unknown current source except the opto-current in the input, such as the leakage current originating from ESD device, will contaminate the output voltage. For these reasons, ESD device is excluded from protecting the CTIA input port.

3. Experiment

A ESD device free CTIA circuit is designed and fabricated with 0.18 µm CMOS process, the microphotography of the chip and the test PCB are presented in Fig. 2(a). To
measure the CTIA circuit, as is shown in Fig. 2(b), the dc voltage generated by the Tektronix AFG3252 is converted to the current with the on-board resistor, which is then injected into the chip, and the output voltage from the CTIA circuit is captured with the Tektronix oscilloscope DPO3054. The pulse control signal is also generated with AFG3252. The captured waveforms in Fig. 3 show the current integration function of the chip. The current flows off the chip, therefore the output voltage ramps up. It’s obvious that the larger the injected current, the faster the voltage ramp.

To observe the soft failure problem that will happen in the ESD device free CTIA circuit, a validation experiment is proposed. In the ESD setup mode, The HBM model is chosen to imitate the ESD event that might be encountered in the CTIA circuit [23, 24]. Instead of using the standard HBM model such as IEC64000-4-2 directly, a minor modification is made. The peak pulse voltage is limited around 200v for the reason that in the Lightly Doped Drain (LDD) CMOS technology, the n-drain region corresponding to the reset switch has low ESD threshold [10].

After one specific ESD event is applied, the current integration function is validated in the measurement mode. It is evaluated constantly after each ESD pulse with different peak voltage is injected into the input terminal of the chip. Fig. 4 shows the normalized slope of CTIA output voltage after different ESD events from two prototyped chips. As in the left figure, when the voltage approach 198v, each time the larger ESD pulse event is applied, the slope of the output voltage is increased. But when the voltage exceeds 222v, the slope decrease to zero abruptly, the chip fails to work completely. In the right figure, although the threshold voltages for the different regions is not exactly the same, it exhibits similar behaviour.

From the proposed experiment, it is obvious that before the chip is completely destroyed by the ESD event, there exists an non-destructive operation region, in which the current integration function is maintained with degraded performance. We, therefore, can define this region as soft failure region.

4. Analysis

By analyzing the CTIA circuit, there exists three possible leakage current paths: path through the gate terminal of the input transistor in the amplifier, the top-plate terminal of the integrating capacitor, and the source terminal of the switch transistor. In theory, the first two leakage paths are contributed by oxide rupture, while the latter is mainly due to the snapback of the parasitic bipolar transistor formed by source, drain and substrate [25, 26].

The increased output voltage slope after the ESD event implies the increased integration current. Therefore, the induced leakage current also flows toward the ground as the input current source. After the prototype chip lose its integration function, the output voltage always clamp to the reset voltage, working as if a unit gain amplifier is formed.
From these two observations, the assumption that the switch transistor is the critical device susceptible to ESD soft failure can be drawn with a simplified model as shown in Fig. 5. In the process of avalanche breakdown, the localized leakage paths is formed in the source/substrate PN junction of the switch transistor under the relatively small ESD event. As the ESD pulse voltage increase further, the short circuit between the source and drain is formed because of strong localized heating, the current integration function can no longer be recovered.

To identify the exact location of the leakage current, we have characterized the CTIA circuit by means of emission microscopy (EMMI) measurements which have been used extensively [27, 28, 29, 30]. The left picture in the Fig. 6 presents the enlarged EMMI image taken after the nondestructive ESD event is applied. The new hot spot as marked with the red circle emerges compared with the previous one (not shown here) taken before any ESD event happens. By crossing check the location with layout picture on the right side, it’s confirmed that there truly exists the leakage path beneath the switch transistor.

5. Conclusion

In this letter, a validation experiment of the soft ESD failure is designed and presented. The CTIA circuit used in the hybrid integrated infrared sensor is chosen as the experimental target, because it’s ESD-protection-device-free, and susceptible to leakage current problem. The experiments shows that under the ESD event with the increased pulse voltage, the induced leakage current increase as well. When the pulse voltage exceeds one certain threshold point, the CTIA circuit fails to work anymore. The subsequent EMMI measurement helps to demonstrate the existence and location of the leakage path.

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References


