LETTER

SPICE simulation of 32-kHz crystal-oscillator operation based on Si tunnel FET

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Abstract The tunnel field-effect transistor (TFET) is one of the promising transistors which is expected to replace some complementary metal-oxide semiconductor (CMOS) circuits. Here, we apply a SPICE simulation of a Si TFET using high-K gate insulator to a simple circuit of 32-kHz crystal oscillator and compare the power consumption of Si TFET with conventional CMOSs calculated from the predictive transistor model (PTM). We considered $L = 65$ -nm and $L = 90$ -nm devices based on a table model whose values are derived from technology computer aided design (TCAD) calculations. We show that the power consumptions of TFETs are about 22.3%~38.6% lower than those of CMOSs for $L = 65$ -nm devices, and we show the 13.6%~36.1% lower power consumption of TFETs for $L = 90$ -nm devices.

Keywords: tunnel field-effect transistor (TFET), crystal oscillation, CMOS, IoT

Classification: Electron devices, circuits and modules

1. Introduction

The era of the Internet of Things (IoT), where many electronic appliances are connected to one another through the Internet, is fast approaching-and with it comes the need for lower power consumptions by electronic circuits and devices. Although the lower supply voltage V_D leads to a quadratic reduction of dynamic power consumption, a simple reduction of V_D results in the reduction of the threshold voltage with an exponential increase of leakage current. This trade-off between V_D and V_{th} restricts the power reduction of the conventional CMOS devices. In order to achieve the low V_D operation, a steeper sub-threshold swing (S.S.) than the conventional CMOS is required. The tunnel field-effect transistor (TFET) is one of such promising devices that has a steeper S.S. less than 60 mV/decade of conventional transistors, by using high-energy filtering effects of the band-to-band tunneling (BTBT) mechanism [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12].

Numerous studies have been conducted to demonstrate the advantage of TFETs by using circuit simulations as well as building device structures with various materials. Mukundrajan *et al.* [13] calculated the circuit performances

of NAND, OR, and other novel circuits, and demonstrated a considerable improvement in the delay and power consumption of TFETs compared with those of FinFETs. Their model is based on Verilog-A model employing GaSb/InAs heterojunction, and therefore a high I_{on} current is expected. Pan *et al.* [14] compared the circuit performance with neuromorphic computing. TFETs such as two-dimensional heterojunction interlayer TFET (thinTFET) [15] exhibited outstanding characteristics even in non-Boolean circuits. There are also many other approaches to constructing TFETs [16, 17, 18, 19]. These investigations revealed that, in order to obtain a low I_{off} with a high I_{on} that is compatible with that of advanced silicon-based devices such as FinFET, various novel structures and materials other than silicon are preferable [20]. However, when we remember that low-cost production is required for IoT devices and that this requirement is different from that of the high-performance devices as used in data centers, it becomes desirable to manufacture TFETs from silicon [21]. In addition, IoT devices spend most of their time in idling or standby states, so it can be said that the high I_{on} is not a significant issue for IoT devices. Even the slightest lower power operation consumes battery energy. Thus, the Si TFETs may be a promising candidate for TFETs if we limit their usage to specific circuits in the low-cost applications. One of such circuits is the 32-kHz crystal-oscillator circuit that generates a conventional clock for each circuit. (32 kHz is a power of 2 ($32768 = 2^{15}$) value, and a precise 1 second period (1 Hz frequency) is obtained by using a 15-stage binary counter.) In Ref. [22], we demonstrated numerically that the power consumption of a 32-kHz crystal-oscillator of TFET is lower than those of low-power CMOSs of $L = 120$ nm, by using a compact model based on the BTBT mode. Because TFETs have device structures different from conventional transistors, the capacitance profiles are also different from those of conventional transistors [23]; therefore, the simulations based on a TCAD model are desirable. In addition, in Ref. [22], we examined only the $L = 120$ -nm devices; therefore, we must also investigate how the lower power consumption TFET changes according to the transistor size. In Ref. [24], we also simulated a Si TFET using high-K materials by using TCAD models. In this paper, we investigate the Si TFET using a table model for $L = 65$ nm and $L = 90$ nm by comparing their counter part of conventional CMOS based on the Predictive Transistor Model (PTM) [25].

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2. Si TFET

The Si TFET in this paper has a pocketless structure where the equivalent oxide thickness (EOT) of the gate oxide is reduced to 0.29 nm. We reached this device structure by starting from the basic structure of the Si TFET. General planar TFETs have a doping gradient in the source region, which causes a spread of the BTBT turn-on gate bias. The spread of the BTBT currents reflects different doping profiles and increases the S.S. to more than 60 mV/decade [26]. Thus, it is difficult to obtain a high on-state current due to the BTBT generation in a local small area in the structure. To solve this problem, the formation of a pocket region with polarity opposite to the source region has been proposed by simulation studies in conventional Si TFET (Fig. 1(a)) [5, 6]. Because the pocket can keep a high electric field at the source-pocket junction as a result of the built-in potential, the rapid rise of source-to-pocket BTBT current at the turn-on voltage is realized and a steep S.S. of less than 60 mV/decade is expected. The tunneling direction in devices is perpendicular to the gate and these types of TFETs are called as vertical TFETs (VTFETs). However, it is difficult to fabricate this structure. In order to increase the gate controllability, the source-pocket junction depth must be ultra-shallow. For example, if the pocket junction depths is larger than approximately 3 nm, the drive current will be seriously reduced, as shown in Ref. [26]. Hence, a low-energy implantation process is needed, which is difficult to achieve. Taking into consideration the thermal process of dopant diffusion, the formation of this kind of shallow pocket region is a challenging problem. In addition, we noticed that an EOT scaling of Si TFETs improved their device characteristics as shown in Refs. [27, 28], and we demonstrated numerically that the pocketless structure (Fig. 1(b)) improved the S.S. of Si TFETs as shown in Ref. [24].

In this paper, we conducted SPICE simulations to determine the performance of a 32-kHz crystal oscillation circuit. The table models for $L = 65$ -nm and $L = 90$ -nm TFETs were generated using TCAD simulations similar to Ref. [24], such that S.S. becomes as small as possible. The device parameters are presented in Table I, in which L_{ov} is gate-to-source overlap length. As shown in Ref. [24], a L_{ov} that is too long might decreased the I_{on} , because of an increase in the source resistance. The table models were embedded into the Verilog-A in the SPICE simulations. We compared the power consumption of TFETs with those of CMOSs whose models were derived from the PTM [25]. In order to fairly compare TFET and CMOS performances, we used the same area and speed for both devices. Because the original CMOS models of $L = 65$ nm and $L = 90$ nm in PTM had much higher speeds than those of TFETs, we

used higher threshold voltage for CMOSs such that the speed of TFETs had a similar order to that of CMOSs. The speeds of the transistors were estimated by using ring oscillators with an even number of inverters with a NAND component (Fig. 2).

3. Basic characteristics of TFETs and CMOSs

As mentioned in the previous section, we reduce the speed of CMOSs by increasing the threshold voltage of the CMOS model. Figs. 3(a)–(d) show the outputs of TFET and CMOS ring oscillators. The threshold voltages of the CMOSs were determined by comparing these oscillation periods. The resultant threshold voltage of the 90-nm CMOS was 0.463 V and that of the 65-nm CMOS was 0.49 V. Figs. 4 and 5 show the I_D - V_G characteristics of pTFET and nTFET with nMOS and pMOS. An average S.S. was determined by the S.S. between $V_{GS} = 0$ and 0.3 V, while the average S.S. of the $L = 65$ -nm device was given by 50.6 nmV/decades and that of the $L = 90$ -nm device was given by 52.8 nmV/decades. As can be seen, the I_{off} s of TFETs of both $L = 65$ nm and $L = 90$ nm are smaller than those of CMOSs at both $V_D = 0.3$ V and $V_D = 50$ mV. On the other hand, although the I_{on} s of TFETs are on the same order as those of CMOSs at $V_D = 0.3$ V (Fig. 4), the I_{on} s of n-type TFETs are smaller than those of CMOSs at $V_D = 50$ mV (Fig. 5). In both regions of V_D , the slope of the I_D - V_G curves of TFETs are steeper than those of CMOSs. This slope is considered to be related to the amplifying ability of the circuits, because the amplifying ability is in proportional to the transconductance g_m , and the slope of the inverter characteristics becomes larger when g_m is large. The gate-to-drain capacitance C_{gd} and the gate-to-source C_{gs} are calculated from the TCAD simulation as in Ref. [24] and taken into the table model of Verilog-A. Fig. 6 shows the C_{SG} - V_D and C_{DG} - V_D characteristics of nTFET and pTFET of $L = 65$ nm which are used in the present table model. The corresponding capacitances of CMOS models are used in the range of PTM model. For TFETs, the tunneling current through the gate oxides are not included assuming an ideal gate stack whose leak current is negligible. Fig. 7 shows the response of NAND circuit for EN = 1 (Enable is ON) which is equivalent to an inverter performance. As the slope of the response increases, as shown in Fig. 7(a)(b), the amplifying ability of the NAND component also increases. We

Fig. 1. TFET device structures. (a) Vertical structure (b) Pocketless structure.

Fig. 2. Ring oscillators consisting of a NAND and two inverters (ro3).

Table I. Device parameters of pocketless Si TFET.

	$L = 65$ nm	$L = 90$ nm
EOT [nm]	0.29	0.29
L_{ov} [nm]	52	77
Source concentration [cm^{-3}]	$7.5\text{e}+19$	$7.5\text{e}+19$
Drain concentration [cm^{-3}]	$1.0\text{e}+20$	$1.0\text{e}+20$
Substrate concentration [cm^{-3}]	$5.0\text{e}+17$	$5.0\text{e}+17$

consider that the slopes of TFET NAND output, which are larger than those of CMOS NAND output, leads to effective generation of oscillations and low power consumption of crystal-oscillators as shown below. From Fig. 7(c) and (d), the through-currents of TFETs in the NAND circuit are much lower than those of CMOSs. This means that the resistances of TFETs are higher than those of CMOSs, as shown in Fig. 4 and Fig. 5. The slight change of the threshold voltage does not significantly affect our results regarding the 32-kHz crystal-oscillator operations, and we do not fine-tune the threshold voltage in this paper. In the following, it will be shown that the power consumptions of TFETs are not so much lower than those of CMOSs. These points will be discussed in later sections.

4. 32-kHz crystal-oscillator operation

Because there are many parameters, even in a simple circuit of crystal-oscillator, we prepared the three datasets. Table II shows the three types of parameter sets for examining the performance of crystal-oscillators in TFETs and CMOSs. The parameters were chosen such that they are in the same order of the magnitudes with widely used models obtained from published data sheets. The calculations show that, as the capacitance C_1/C_0 increases or W increases, the oscillation stabilizes. Thus, first we chose C_0 and increased C_1 or W gradually. In Table II, C_1 s were chosen as smallest as possible such that the 32-kHz oscillations were observed when C_0 and W are given. The parallel resonant frequency f_p and the series resonant frequency f_s are defined by $f_s = \frac{1}{2\pi\sqrt{L_1C_1}}$, and $f_p = \frac{1}{2\pi\sqrt{L_1C_0C_1/(C_0+C_1)}}$. We found that, as C_1/C_0 increased, the difference between f_p and f_s became greater. The circuit capacitances (pF order) described in Table II are larger than the device capacitances shown in Fig. 6. Thus, it can be said that the detailed capacitance characteristics of the TFETs (Fig. 6) will not significantly affect the circuit performance.

Fig. 9 shows the 32-kHz crystal oscillation using 65-nm TFETs and CMOSs for $V_D = 0.3$ V and 0.4 V. When the results of TFETs were compared with those of CMOSs, the amplitudes of the outputs of TFETs were slightly larger than those of CMOSs. This is considered to be the result of the Miller effect [29] as discussed in Ref. [22]. Fig. 10 shows the corresponding current through the oscillation circuits. The current is numerically monitored at the drain voltage of the NAND circuit. We can see that the amplitudes of currents of the TFETs were about a half of those of the CMOSs. These lower currents result in lower power consumption. Table III shows the average power consumptions of both TFETs and CMOSs, where the currents are averaged after the oscillations stabilize from Fig. 10. It is proven that the power consumptions of TFETs are about 22.3%~38.6% lower than those of CMOSs.

For $L = 90$ nm, similarly to the results of $L = 65$ nm cases, we can see the increase of the output amplitudes of TFETs compared with those of CMOSs and the lower power consumption of TFETs. Table IV shows the average power consumptions of both TFETs and CMOSs, and we can see the 13.6%~36.1% lower power consumption of

Fig. 3. Simulation of ring oscillators consisting of a NAND and two inverters (Fig. 2, ro3) and a NAND and ten inverters (ro11). (a) TFET of $L = 65$ nm (b) CMOS of $L = 65$ nm based on PTM where $V_{th} = 0.463$ V. (c) TFET of $L = 90$ nm (d) CMOS of $L = 90$ nm based on PTM where $V_{th} = 0.49$ V.

Fig. 4. I_D - V_G characteristics of TFET and CMOS at $V_D = 0.3$ V. (a)(b) TFET and CMOS of $L = 65$ nm (c)(d) TFET and CMOS of $L = 90$ nm. TFET parameters were calculated as in Ref. [24]. CMOS parameters were obtained from PTM [25] such that the speed of ring oscillators had the similar periods as those of TFETs.

Fig. 5. I_D - V_G characteristics of TFET and CMOS at $V_D = 50$ mV. (a)(b) TFET and CMOS of $L = 65$ nm (c)(d) TFET and CMOS of $L = 90$ nm. TFET parameters were calculated as in Ref. [24]. CMOS parameters were obtained from PTM [25] such that the speed of ring oscillators had the similar periods as those of TFETs.

Fig. 6. The gate-to-source Capacitance C_{gs} - V_D and the gate-to-drain Capacitance C_{gd} - V_D characteristics of nTFET and pTFET of $L = 65$ nm devices calculated TCAD simulation as in Ref. [24]. We have similar characteristics for $L = 90$ nm devices.

Fig. 7. Output of NAND circuits of TFETs and CMOSs. (a) Output voltage of $L = 65$ nm. (b) Output voltage of $L = 90$ nm. (c) Output current of $L = 65$ nm. (d) Output current of $L = 90$ nm.

Fig. 8. (a) Crystal-oscillator circuit. (b) Equivalent circuit of quartz crystal using four elements.

Table II. Parameters in crystal oscillator circuit

	Dataset A	Dataset B	Dataset C
W [μm]	5	10	16
C_0 [pF]	0.9	1.2	2.5
C_1 [pF]	0.3	0.3	1.2
L_1 [H]	85	102	28
R_1 [kΩ]	5	5	5
C_2 [pF]	0.6	0.6	1
C_3 [pF]	0.6	0.6	1
R_3 [MΩ]	1000	1000	1000
R_4 [kΩ]	100	100	100
R_5 [kΩ]	25	25	25
f_s [kHz]	28.77	29.97	27.46
f_p [kHz]	33.22	33.51	33.40

Table III. Comparison of power consumption of 65 nm TFET model with 65 nm CMOS model

	DatasetA		DatasetB		DatasetC	
V_D	0.3 [V]	0.4 [V]	0.3 [V]	0.4 [V]	0.3 [V]	0.4 [V]
TFET [nW]	1.13	3.14	0.57	2.15	1.24	4.30
CMOS [nW]	1.83	4.40	0.91	2.77	1.82	6.17
Ratio [%]	61.42	71.39	63.23	77.68	68.08	69.68

TFETs. Table III and IV are plotted in Fig. 12. From Table III and Table IV, TFETs exhibit less effective compared with CMOSs. In addition, in both Table III and Table IV, the results of $V_D = 0.4$ V show greater power consumption than those of $V_D = 0.3$ V.

This might be partly because the doping concentrations of Table I were determined by minimizing the S.S. of $L = 1$ μm in Ref. [24]. The L_{ov} of $L = 65$ nm and $L =$

90 nm were optimized by fixing the three doping concentrations. However, V_D dependence is not well understood at present. There are many parameters in the crystal-oscillator circuit, and it is considered that each device has its own optimal characteristics, depending on V_D . In order to compare different devices, we have to fix most of their parameters for fair comparisons. Thus, it is possible that one parameter set which is best for one device may not be best for other devices. This is a problem that will require future investigation. In any case, it is expected that the power consumption of TFET is lower than that of CMOSs. It appears that the power reductions of TFETs in Tables III and IV are not as large as predicted by the through-current reductions shown in Fig. 7(c) and (d). It is considered that this is the results of the polarity of the current oscillations polarities shown in Fig. 10. The currents of TFETs generally have the same polarities. On the other hand, the CMOS currents have both positive and negative polarities. In the NAND gate shown in Fig. 8, the opposite current means that the oscillating circuit generates electric power. Let us consider the reason why there is smaller opposite current flow in TFETs by regarding the NAND circuit as an inverter. The opposite currents flow when the output voltage of the inverter is higher than the drain voltage of pMOS at $V_D \leq 50$ mV. This is in the case of Fig. 5. We therefore deduced that the higher resistance of TFETs (clear low I_{off}) blocks the backward current from the LCR circuit of the part of Fig. 8 to the power source. Thus, although the currents through the NAND gate shown in Fig. 7 of CMOSs are much larger than those of TFETs, the final power consumptions of TFETs are not so large. Finding the appropriate I - V characteristics suitable for a 32-kHz crystal-oscillator will require future investigation.

5. Oscillation margin

Let us check the stability of the oscillations. The oscillation margin was estimated by checking whether the oscillation is possible when R_5 increases. The oscillation margin M_{osc}

Fig. 9. Output of 32-kHz oscillation of $L = 65$ nm when V_D is changed. (a) TFET of dataset A, (b) CMOS of dataset A, (c) TFET of dataset B, (d) CMOS of dataset B, (e) TFET of dataset C, (f) CMOS of dataset C.

Fig. 10. Current through the circuit of the 32-kHz oscillation of $L = 65$ nm when V_D is changed. (a) TFET of dataset A, (b) CMOS of dataset A, (c) TFET of dataset B, (d) CMOS of dataset B, (e) TFET of dataset C, (f) CMOS of dataset C.

Table IV. Comparison of power consumption of 90 nm TFET model with 90 nm CMOS model

	DatasetA		DatasetB		DatasetC	
V_D	0.3 [V]	0.4 [V]	0.3 [V]	0.4 [V]	0.3 [V]	0.4 [V]
TFET [nW]	1.33	3.92	2.27	7.18	1.31	5.24
CMOS [nW]	2.08	4.64	3.15	8.32	1.91	6.67
Ratio [%]	63.95	84.38	72.12	86.36	68.58	78.50

Fig. 11. Output of 32-kHz crystal-oscillator of $L = 65$ -nm TFET and CMOS for $V_D = 0.3$ [V] when R_5 is changed to examine the oscillation margins. (a) TFET of Dataset A, (b) CMOS of Dataset A, (c) TFET of Dataset B, (d) CMOS of Dataset B, (e) TFET of Dataset C, (f) CMOS of Dataset C.

is defined from the load resonance frequency f_L , the load resistance R_L , and the load capacitance C_L , which were given by $f_L = f_s(C_1/[2(C_0 + C_1)] + 1)$, $R_L = R_1(1 + C_0/C_L)^2$, and $C_L = (C_1/2)/(f_L/f_s - 1) - C_0$ [30]. The calculated values are listed in Table V. The oscillation margin degree was given by $M_{osc} \equiv R_5/R_L$. The general condition

Table V. Load capacitances, load frequency and load resistance of the oscillation circuits

	Dataset A	Dataset B	Dataset C
C_L [pF]	0.3	0.3	1.2
f_L [kHz]	32.37	32.97	31.91
R_L [kΩ]	80	125	47.53

Fig. 12. Table III and IV are illustrated. (a) Power consumptions of the 32 kHz oscillation for 65 nm TFETs and CMOSs, as a function of V_D , and (b) those for 90 nm devices. (c) Ratios of the power consumption of TFETs over CMOSs. 'A', 'B', and 'C' show 'Dataset A', 'Dataset B', and 'Dataset C', respectively.

of the stable oscillation is considered to be given by $M_{osc} \geq 5$. Fig. 11 shows the numerical results of the 32-kHz oscillations when R_5 increased to meet the condition of the oscillation margin ($M_{osc} \geq 5$). As can be seen, as R_5 increased, the amplitudes of oscillation were inclined to the decreases in the devices of the datasets A and C. In contrast, the oscillations were stable for the devices of the dataset B devices. Thus, it is confirmed that the oscillation margin depends on parameter regions.

6. Conclusion

We calculated the power consumption of a TFET based on the TCAD table model for an application of 32-kHz crystal-oscillator circuits. We compared the power consumptions of 65-nm and 90-nm TFETs with those of CMOS based on the PTM model under the conditions of equal area and speed. We showed that the power consumption of TFETs is smaller than those of CMOSs for several circuits. The origin of this low power consumption of TFETs comes from the low I_{off} and the steeper S.S. of TFETs, which induces a larger amplification of signals in the 32-kHz crystal-oscillator circuits. The disadvantage of using TFET would be an extra cost of fabrication because the circuits other than the crystal-oscillator are made by conventional transistors. The trade-off between the lower consumption and the extra fabrication cost would be a future problem.

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