LETTER

Substrate effect on radiation-induced charge trapping in buried oxide for partially-depleted SOI NMOSFET

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Abstract The total-ionizing-dose response of partially-depleted silicon-on-insulator devices with or without grounded substrate under different irradiation bias is investigated. Compared with devices with grounded substrate, the devices with floating substrate introduces more trapped positive charges in buried oxide after irradiation, leading to larger negative shift of back-gate threshold voltage, especially for ON bias condition. Theoretical analysis and TCAD simulation demonstrate that, this phenomenon is attributed to the increased initial built-in field in buried oxide and weakened space charge effect under the case of floating substrate. According to this work, substrate terminal of SOI devices must be considered for integrated circuit design under radiation condition.

Keywords: total-ionizing-dose, partially-depleted SOI, buried oxide, floating substrate

Classification: Electron devices, circuits and modules

1. Introduction

Nowadays silicon-on-insulator (SOI) technology has been widely applied for its intrinsic potential advantages over bulk-Si technology, such as high performance and low power circuits. In particular, owing to better resistance against transient ionization effects SOI technology has wide application in harsh radiation environment [1, 2, 3, 4, 5]. However, the thick buried oxide (BOX) layer threatens the reliability of SOI devices during ionizing radiation, in which the positive trapped charges will build up in the BOX after total ionizing dose, reducing the threshold voltage of back-gate transistor and increasing leakage current [6, 7, 8, 9]. The radiation response of buried oxides has been found to be highly dependent on the device bias configuration during radiation, which determines the electrical field distribution in BOX [10, 11, 12, 13, 14, 15, 16, 17, 18].

The impacts of substrate bias on radiation response of partially-depleted (PD) SOI devices have been investigated [19, 20, 21, 22, 23, 24]. In [24], for SOI NMOS negative voltage at back-gate transistor can reduce the number of positive charges trapped in BOX during irradiation, eliminating the back-gate effect on front-gate transistor's performance. However, the research about influence of float-

ing substrate on total-ionizing-dose (TID) response of PDSOI devices is relatively limited. In some specific application, especially for Radio-Frequency (RF) circuits with high-speed requirement, the substrate terminal of packaged SOI devices is required to be floating in order to reduce the loss and parasitic capacitance of substrate. Besides, there is no unified rule about whether or not the substrate of PDSOI devices is grounded during TID research. Hence, investigating the floating substrate effects on TID response of PDSOI devices is necessary. In this paper, packaged PDSOI devices with grounded or floating substrate were submitted to radiation environment under different bias conditions. We observed that, compared with devices with grounded substrate, those devices with floating substrate display larger negative shift of back-gate threshold voltage after irradiation, especially under ON bias. Both physical mechanism and TCAD simulation were put forward to explain this phenomenon.

2. Experimental details

The PDSOI devices used in this work were fabricated by 130 nm PDSOI CMOS technology. The SOI material was from SOITEC Corporation's 200 mm diameter UNIBOND wafer with a 100 nm thick Top-Si film and a 145 nm thick BOX. The input/output (I/O) NMOS with $W/L = 10 \mu\text{m}/0.35 \mu\text{m}$ was selected. The gate oxide thickness is about 6 nm and the operating voltage (V_{DD}) is 3.3 V. We adopted the H-shape gate device, as depicted in Fig. 1, to avoid the influence of shallow trench isolation on device during radiation [25, 26]. The devices were 24-pin DIP ceramic packaged.

We carried out this experiment in Xinjiang Technical Institute of Physics and Chemistry, the Chinese Academy of Sciences. The radiation source was ^{60}Co γ -ray and the dose rate was 200 rad(Si)/s. During radiation exposure, the devices were irradiated up to 500 krad(Si) under different bias conditions as displayed in Table I. We periodically interrupted the irradiation to measure the DC characteristics of the devices using Keithley 4200B parameter analyzer at room temperature. The threshold voltage is extracted by the constant current method according to I_d - V_g characteristics. The threshold voltage of front or back gate transistor is defined when the drain current reaches $(W/L) \times 10^{-7}$ A at a drain voltage of $V_d = 0.1$ V. Three test samples were used for every radiation bias condition, on top of that, to ensure the repeatability this experiment has been conducted several times, which showed the same result.

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Fig. 1. Schematic top-view (top) and cross-section (bottom) of H-gate PDSOI NMOSFETs

Table I. Bias conditions under irradiation of the PDSOI I/O NMOS. The substrate of devices are grounded with 0V, or Floating.

Bias	Source	Drain	Gate	Body	Substrate
ON	0 V	0 V	V_{DD}	0 V	0 V
ON-F	0 V	0 V	V_{DD}	0 V	Floating
PG	V_{DD}	V_{DD}	0 V	0 V	0 V
PG-F	V_{DD}	V_{DD}	0 V	0 V	Floating
0V-F	0 V	0 V	0 V	0 V	Floating

3. Experimental result and discussion

Fig. 2 and Fig. 3 show TID response of H-gate PDSOI I/O NMOS ($W/L = 10 \mu\text{m}/0.35 \mu\text{m}$) under ON and ON-F bias respectively. In general, due to the existence of body contact, which functions as the substrate in bulk silicon technology, for PDSOI devices the substrate terminal does not have influence on DC electrical characteristics of front-gate transistor. As illustrated in Fig. 2, before irradiation the curve of device with floating substrate overlaps the curve with grounded substrate. However, there is appreciable difference after TID effect. When the device with grounded substrate has negligible leakage current after 500 krad(Si) irradiation, obvious off-state leakage current of front-gate transistor has already happened after 300 krad(Si) in the case of device with floating substrate. From Fig. 3, we observe that the device with floating substrate has larger negative threshold voltage shift of back-gate transistor than that of device with grounded substrate after irradiation. Furthermore, the subthreshold region of device with floating substrate crosses over zero voltage when total dose is up to 300 krad(Si), which results in the large leakage current in front-gate transistor. It is indicated that the substrate state affects the TID response of BOX.

Fig. 2. Front-gate I_{ds} - V_{FG} transfer characteristic of H-gate PDSOI I/O NMOS ($W/L = 10 \mu\text{m}/0.35 \mu\text{m}$) under ON and ON-F irradiation bias at different total dose levels.

Fig. 3. Back-gate I_{ds} - V_{BG} transfer characteristic of H-gate PDSOI I/O NMOS ($W/L = 10 \mu\text{m}/0.35 \mu\text{m}$) under ON and ON-F irradiation bias at different total dose levels.

To the best of our knowledge, radiation produces electron-hole pairs in the oxide layer. Under the electrical field, some created electrons and holes escape the initial recombination. Most of separated electrons will rapidly drift away from the oxide, and a fraction of separated holes will be trapped during transporting toward the Si/SiO₂ interface, resulting in the positive trapped charges and interface defects buildup [2, 27, 28]. In order to analyze the substrate effects on charge trapping process in buried oxide during irradiation, SOI devices are submitted to total dose radiation under different bias conditions. Using the method introduced in [29], the effective sheet charge density of the oxide trapped hole (N_{ot} , positive charge) and the interface traps (N_{it} , negative charge) under different bias conditions after 300 krad(Si) and 500 krad(Si) irradiation are extracted. (We assume the N_{ot} and N_{it} are zero before irradiation). According to the results shown in Table II, both the oxide trapped charge and the interface traps increase with total dose and N_{ot} is nearly one order of magnitude larger than N_{it} , which confirms that the radiation-induced trapped positive charge in the BOX is the decisive factor for the variation of back-gate threshold voltage. Fig. 4 illustrates the shift of the back-gate thresh-

Table II. The effective sheet charge density of the oxide trapped charges (N_{ot}) and interface traps (N_{it}) under different bias after irradiation

TID	300 krad(Si)		500 krad(Si)	
Bias	N_{it}/cm^{-2}	N_{ot}/cm^{-2}	N_{it}/cm^{-2}	N_{ot}/cm^{-2}
ON	3.2×10^{10}	8.9×10^{11}	1.2×10^{11}	1.0×10^{12}
ON-F	1.1×10^{11}	1.4×10^{12}	1.8×10^{11}	1.6×10^{12}
PG	5.2×10^{10}	1.7×10^{12}	1.6×10^{11}	1.8×10^{12}
PG-F	7.3×10^{10}	1.7×10^{12}	1.9×10^{11}	1.9×10^{12}
0V-F	1.3×10^{11}	1.4×10^{12}	1.5×10^{11}	1.5×10^{12}

old voltage under different irradiation bias. Interestingly, the 0V-F bias has similar shift value with the ON-F case, which demonstrates that the charge trapping in BOX is not influenced by the gate bias during irradiation [10, 12]. As expected, the PG bias condition, the worst irradiation bias for back channel [10, 12, 17], introduces much larger negative threshold voltage shift than that of ON bias. However, different from the ON case group, there is no significant difference between the PG bias and PG-F bias.

Fig. 4. Back gate threshold voltage shift versus dose of a H-gate PD SOI I/O NMOS ($W/L = 10 \mu\text{m}/0.35 \mu\text{m}$) under different irradiation bias condition (the solid line indicates experimental result and the dash line indicates simulated result).

Radiation-induced positive charge trapping in BOX is determined by built-in field and space charge effect with increasing total dose [20, 28, 30]. And the capture rate of the positive charge near the Si/SiO₂ interface can be estimated by the following formula [31]):

$$\frac{dN_{ot}}{dt} = (n_t - N_{ot})\sigma_p \cdot |f_p| - R_{N_{ot}} \quad (1)$$

where n_t and σ_p are total hole trapping sites density and hole capture cross section which are related to the process. The recombination factor, $R_{N_{ot}}$, expresses the removal (or compensation) rate of trapped holes from the system. And f_p , the hole flow density, indicates that the holes generated by the irradiation escaped the initial recombination with the symbiotic electrons and drifted towards the Si/SiO₂ interface driven by the electric field and it strongly depends on the electric field strength. In the beginning of irradiation,

under the initial built-in field in BOX, generated holes move toward the Top-Si/BOX interface and are trapped continuously. Furthermore, the larger the built-in field is, the more holes will escape the initial recombination, i.e. larger f_p , and be trapped by oxide defects. As positive charges accumulate in BOX with total dose, the potential of BOX upper interface increases, forming an electrical field pointing to the lower interface. The buildup field from the trapped-hole space charges weakens the built-in field effect and restricts the generation and distribution of holes. Fig. 5 shows schematic representation of built-in field lines and space-charge-induced buildup field lines in BOX of PDSOI NMOSFETs under PG bias. For PG bias condition, the initial built-in electrical field in BOX is mainly attributed to the voltage drop between drain/source and body region, resulting from the intrinsic doping voltage drop and the extrinsic added voltage. The potential difference, up to 4 V under drain-body and drain-source junctions, makes more positive charge trapped near the Top-Si/BOX interface under the body field, leading to obvious negative shift of back-gate threshold voltage. Finally, the space charge effect becomes strong enough when comparable number of holes are trapped, with a result that the back-gate threshold voltage shift reaches saturation. Meantime, according to Eq. (1), in addition to the reduced electric field strength due to the space charge effect, the reduction of the unoccupied hole traps ($n_t - N_{ot}$) can also lead to the decrease of charge capture rate.

Fig. 5. Schematic representation of built-in field lines and space-charge-induced buildup field lines in buried oxide of PDSOI NMOSFETs under PG bias condition.

For ON case, since the Si film is grounded, the initial electrical field in BOX would be only determined by the built-in potential between the p-type Si film and the lower doped p-type substrate [19], which is about 0.2 V, much smaller than the built-in potential of PG bias. As shown in Fig. 6, under the low built-in electrical field in BOX, radiation-induced electrons recombine quickly with the trapped holes, leaving a small number of unremoved holes located near the Top-Si/BOX interface. Furthermore, any charge buildup will radically alter the local oxide fields under very low initial internal field in BOX, hence, the space charge effect plays a major role for charge trapping in the beginning. As shown in Fig. 4, under ON bias the negative shift of back-gate transistor has almost reached saturation when the shift value is only about 5.8 V, smaller than that of PG bias.

Fig. 6. Schematic representation of built-in field lines and space-charge-induced buildup field lines in buried oxide of PDSOI NMOSFETs under ON bias condition.

Fig. 7. Simulated potential in BOX in vertical direction for ON and ON-F bias cases before/after irradiation.

The TCAD simulated potential and electric field in BOX for different bias cases before and after irradiation are shown from Fig. 7 to Fig. 10. The irradiated situation was carried by setting uniform positive charge at the upper interface of the BOX and the surface density of each case is marked as N_{ot} in these figures. It should be noted that we have changed the charge density as the data in Table II and compared the simulated results of $\Delta V_{t,bg}$ with the experiment results. And they showed good agreement, which indicates that the simulation is reliable. From the simulation results of ON and ON-F bias from Fig. 7, before the irradiation, when the substrate is floating, the electrical potential difference between the lower and upper interface of the BOX reaches about 0.4 V, which nearly doubles the built-in electric field in BOX compared to the grounded substrate condition, as shown in Fig. 8. For ON and ON-F bias, the electric field in the BOX is mainly perpendicular to the interface and the holes are separated and driven to the upper interface by the negative vertical electric field. The larger vertical electrical field drives more holes to be separated during irradiation. Meantime, different from the grounded substrate, the potential of the floating substrate is more controlled by the nearby buried oxide region. After irradiation, the accumulated holes at the upper interface of the BOX can generate the electric field from the upper interface to the lower interface (i.e. space charge electric

Fig. 8. Simulated build-in vertical electric field in BOX in vertical direction for ON and ON-F bias cases before/after irradiation.

Fig. 9. Simulated space charge vertical electric field in BOX in vertical direction for ON and ON-F bias cases after irradiation.

Fig. 10. Simulated lateral electric field and potential in BOX along the interface for PG and PG-F bias cases before/after irradiation.

field), partially offsetting the built-in electric field, which from the bottom to the top. As we can see from Fig. 7, when the spacing charge effect, induced by the same surface charge density ($N_{ot} = 1 \times 10^{12} \text{ cm}^{-2}$), raise the potential of BOX upper interface, the potential of lower interface also increases for both ON and ON-F condition, but the

enhancement of the latter is much larger than the former, seen from the Δ Potential on Fig. 7. Meanwhile, when the surface charge density changes to $1.6 \times 10^{12} \text{ cm}^{-2}$, which corresponding the situation of 500 krad(Si) irradiation dose of ON-F bias, the elevation of the potential at the lower interface is more significant. On the other hand, as shown in Fig. 8, though the vertical electric field in the most areas of the BOX near the lower interface of both ON and ON-F condition is reduced (as shown by the up arrow in Fig. 8), the decreases of the ON-F one is less significant than the grounded substrate whether at the charge density of $1 \times 10^{12} \text{ cm}^{-2}$ or $1.6 \times 10^{12} \text{ cm}^{-2}$, indicating that the floating substrate leads to relatively smaller space charge effect. What's more, until the N_{ot} increases to $1.9 \times 10^{12} \text{ cm}^{-2}$, the vertical electric field near the lower interface drops to approach the un-irradiated ON bias situation. Meantime, as we can see from Fig. 4 and Table II, the trapped positive charge density is close to saturation at around $1.6 \times 10^{12} \text{ cm}^{-2}$, which means that the vertical electric field in the BOX under the ON-F bias will always be larger than the ON bias. In other words, the electric field is not the reason to limit the continued capture of charge for ON-F bias condition. As will be mentioned later, the total hole traps density in the buried oxide (n_t) is about $2 \times 10^{12} \text{ cm}^{-2}$. Therefore, when the trapped charge density N_{ot} is $1.6 \times 10^{12} \text{ cm}^{-2}$, most of the hole traps have been occupied, and the reduction in unoccupied hole traps is the cause that leads the saturation. In order to demonstrate this weakened space charge effect more intuitively, we extracted the space charge effect induced electric field by subtracting the total vertical electric field after irradiation from that before irradiation and plot it in Fig. 9. As we can see from it, the space charge electric field of ON-F bias at the charge density of $1 \times 10^{12} \text{ cm}^{-2}$ even $1.6 \times 10^{12} \text{ cm}^{-2}$ is significantly smaller than ON bias. In summary, the larger potential enhancement and the accompanying smaller electric field decrease can be attributed to the weakened space charge effect after irradiation. And, the enhanced radiation degradation for devices with the floating substrate is due to the increased built-in field and weakened space charge effect and the saturation of the degradation is due to the reduction of the unoccupied hole traps.

For PG and PG-F bias cases, the peak value of the electric field in the BOX appears at the upper interface near the source/body or drain/body junction, which pushes the hole laterally into the center region. Thus we plot the potential and the lateral electric field along the channel direction at 10 nm below the upper interface, as illustrated in Fig. 10. The incremental voltage drop between the two interfaces of BOX due to the floating substrate has a negligible effect on the potential along with the interface and the peak electrical field under two junctions, which dominate the charge trapping under PG bias during radiation. Since the initial voltage drop between source/drain and body region is large, the relatively small variation of the potential difference due to the floating substrate has a non-significant impact on charge trapping during irradiation, so as the space charge effect. What's more, because the electrical field does not change much when the trapped charge density reaches $1.9 \times 10^{12} \text{ cm}^{-2}$, the saturation of

the degradation can be attributed to the limitation of the number of hole traps. Therefore, we can reasonably speculate that the density of the total hole traps is about $2 \times 10^{12} \text{ cm}^{-2}$, which also explains the saturation happened on ON-F bias condition.

4. Conclusion

In summary, the substrate state has critical impact on charge trapping in BOX during total ionizing dose, especially for those SOI devices under ON case with low initial built-in field in BOX. Compared with grounded substrate condition, the floating substrate increases the trapped positive charges in volume of BOX after irradiation through increasing the potential of substrate and weakening the space charge effect. Concerning PG case, since the holes buildup is mainly attributed to the large voltage drop between source/drain and body region, whether the substrate is grounded or not has non-significant impact on charge trapping during irradiation. Thus, although the floating substrate does not obviously affect the TID effect of PG-biased devices, this paper still revealed the importance of substrate bias to SOI devices in radiation environment, and also provides useful information for integrated circuit design and manufacture that used in space, especially for those circuits that rarely use or without pass-gate transistors.

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