Abstract The adaptive bias technique is the common technology for improving the power-added efficiency (PAE) of the power amplifier (PA). However, the performance of the adaptive bias technique is sensitive to the frequency variation. This paper presents a novel adaptive bias as the common-source bias of the 45–2500 MHz CMOS PA, which combines the subthreshold PD to decrease the effect on frequency of adaptive bias technique and a unity gain amplifier to increase the detection sensitivity, for improving the PAE at back-off mode over the wide bandwidth. The proposed PA provides a good performance from 45 MHz to 2500 MHz, while the peak of the saturation output power is 24.02 dBm over the frequency band. Moreover, the maximum PAE achieves 44.61% at 500 MHz and the PAE is larger than 28.48% at 3 dB back-off power. The chip size of the broadband PA achieves 1.87 mm² at TSMC 0.18 um technology process. It draws 200 mA from 3.3 V supply voltage.

Keywords: adaptive bias technique, broadband PA, efficiency

Classification: Integrated circuits

1. Introduction

Meeting the demands of multiple-wireless communication applications (e.g., software-defined radio), the number of protocols in different frequency bands continue to rise, such as LTE, WCDMA, GSM, WLAN and etc. Integrating these protocols into a single transmitter is of consequently extreme importance [1, 2, 3]. A power amplifier (PA) as the key device of the transmitter, which meets the demands of broadband, is usually integrated on chip to provide high power signal. Meanwhile, the PA always consumes the most direct current power consumption, and its efficiency dominates the lifetime of the battery [4, 5]. So realization a broadband PA with high efficiency is one of the main trends.

There are two solution for realizing CMOS broadband PA. The first way is optimizing the performance of the matching network, which includes switched-capacitor PA [6, 7], transformer-based PA [8, 9] and transmission line PA [10, 11]. But the value of the passive devices and the complexity of the matching network will be enhanced with the bandwidth expanding. The second way is decreasing the influence of the transistors by frequency, such as the cross-coupled structure [12, 13] and the negative feedback structure [14, 15]. However, the bandwidth of the proposed structure cannot be expanded indefinitely.

In order to provide enough power gain, the core of the broadband CMOS PA mentioned above is always much larger than the narrowband PA. The more power consumption of the broadband PA leads to lower efficiency. The PA is usually operated in back-off mode for the digital modulation signal with high peak-to-average power ratio [16]. The power-added efficiency (PAE) at the output power back-off is of consequently extreme importance. Several techniques are used to overcome the low efficiency characteristic of PA at back-off mode. The most popular one for enhancing the efficient of the PA is the supply modulation technique which is not fit for the high speed application [17, 18]. The class-J and class-F enhance the efficiency by the superposition of harmonics and fundamental waves but the proposed structure cannot be used in a PA with a large relative bandwidth [19, 20]. Doherty PA uses active load pull technique for improving the back-off efficiency but the operating bandwidth is limited by the 1/4 transmission line [21, 22]. The adaptive bias technique is used to improve the PAE at the back-off mode and the linearity of the PA at the saturation mode [23]. There are two structures for realizing the adaptive bias technique, which include envelope tracking bias modulator and diode bias technique [24, 25]. However, the structure of the envelope tracking bias modulator is complicated and occupies more chip area. The diode bias technique, which is heavily influenced by frequency, is just used in narrow band application.

In this paper, a novel adaptive bias as the common-source bias of the broadband PA, which combines the sub-threshold power detector (PD) to decrease the effect on frequency of adaptive bias technique, is used in a 45–2500 MHz transmitter for improving the PAE at the output power back-off, and can enhance the linearity of the broadband PA at the high output power. The sub-threshold PD, which combines a unity gain amplifier to enhance the detection sensitivity, is used as the novel adaptive bias structure. Meanwhile, the low output resistance of the unity gain amplifier is easy to drive the large filter capacitance and the large input resistance can improve the isolation of the sub-threshold PD. The paper is organized as follows. A novel adaptive bias and the structure of the sub-threshold PD are described in section 2. The measured results of the broadband PA, which is designed by using the proposed adaptive bias, are demonstrated in section 3. The conclusions are shown in section 4.
2. Novel adaptive bias for broadband PA

The large signal performances of the broadband PA are dependent on bias. Integrated bias can enhance the linearity, which is one of the advantages of the CMOS technology process. However, realizing the broadband PA, which use the CMOS process, is a major challenge. Because the trade-off between the PAE, output power, linearity and bandwidth needs to be considered. To address these limitations, the adaptive bias technique is used for improving the PAE at the back-off mode and the linearity at the saturation mode.

In order to provide a bias which is sensitive to the input power, the PD can be used. The PD provides a bias which changes with the input power. Several techniques are presented for realizing PD, such as Schottky diode detector, root-mean-square (RMS) PD, bipolar transistor (BJT) detector and sub-threshold detector. The properties of the Schottky diode detector [26], which is not the standard device in CMOS technology process, is good in RF band. The RMS PD [27] can achieve wide input dynamic range, but additional coupler costs large chip area and it is sensitive to the frequency. The dynamic range of the BJT PD [28] is high in a wide frequency band. However, it is less compatible with the standard CMOS process. The sub-threshold PD [29] has good performance over frequency variation and will not decreased the output power. It is thus used to provide a bias which is not affected by frequency and fits for the designing of broadband PA at the CMOS process. Meanwhile it is simple, but the narrow output dynamic range will lead to low detection sensitivity.

The traditional sub-threshold PD [29] is plotted in Fig. 1a. The M1 and M2, which implement the power detecting function, are biased in sub-threshold region. The sub-threshold current IDS of M1 and M2 is proved by the current source, so the sum of IDS1 and IDS2 keeps constant.

\[ I_{DS} = I_{DS0} \text{exp}(-V_{th}/nV_{T}) \]  
where \( V_G \) and \( V_S \) are the voltage of the gate terminal and the source terminal, \( V_{th} \) is the threshold voltage and \( n \) is the nonideal factor only related to temperature. The \( V_{out} \) can be determined by the following equation:

\[ V_{out} = \frac{V_{in} + V_{B}}{n} - V_{T} \left( \ln \frac{\sqrt{2\pi V_{in}/nV_{T}}} \right) - \ln \frac{I}{2I_{0}} \]  

\[ V_{T} = \frac{KT}{q} \]  

where \( V_{in} \) is the input voltage swing, \( I \) is the sum of IDS1 and IDS2, \( V_{B} \) is the bias voltage of M1 and M2, \( T \) is the temperature, \( K \) is the Boltzmann constant and \( q \) is the electron charge. The supply voltage keeps constant, so the \( V_{DS} \) of M1 and M2 will be reduced with rising of the input voltage swing \( V_{in} \) and the relationship between the \( V_{DS} \) and \( V_{in} \) is linear. According to (3) and (4), the upper limit value of the sub-threshold PD is lower than the supply voltage, while the lower limit value is large than \( V_{th}/n - V_{T} \left( \ln \sqrt{2\pi V_{in}/nV_{T}} \right) \). The symbols in expressions (1), (2), (3) and (4) are independent of frequency. Thus, the expression (3) can prove that the output voltage of the sub-threshold PD is not affected by frequency.

The novel sub-threshold PD for improving the output dynamic range is shown in Fig. 1b. The transistor M3 and M4 biased in sub-threshold region are used as the input transistor of the unity gain amplifier. According to the equation (3), the \( V_{DS} \) of M3 and M4 will be reduced with rising of the input voltage swing. The voltage of node A is decreased. Meanwhile, the voltage of node B and node C is increased. The voltage of node B and node C can be used as the output voltage of PD and can represent the output voltage of the novel and the traditional structure, respectively. The dynamic range of the node A is expanded by the second stage amplifier of the unity gain amplifier and the feedback circuit decreased the setting time. Thus, the voltage range of node B is larger than the voltage range of node C. The simulation results are plotted in Fig. 2. The output dynamic range of the novel structure is 300 mV larger than the output dynamic range of the traditional one, so the detection sensitivity of the novel structure is enhanced. Because the drain resistance of M6 is much smaller than R5. The low output resistance, which is approximately equal to the drain resistance of M6, of the unity gain amplifier is easy to drive large filter capacitors. The input resistances, which is approximately equal to the gate resistance of M3 and M4, can improve the isolation of the sub-threshold PD.

The linear dynamic range changes from 0.01 V to 1 V equivalent to the input power from -30 dBm to 10 dBm in the whole frequency band. The measured output voltage of the proposed PD versus input voltage swing is demonstrated in Fig. 3 and Fig. 3 can provide the proposed PD has good performance over frequency variation. As shown in Fig. 4, the detection error, which is obtained by comparing with the output voltage at 1250 MHz, is lower than ±0.4 dB from 45 MHz to 2500 MHz.

A 45–2500 MHz PA, which combines the on-chip and the off-chip matching network, needs to be designed for a
A wideband wireless transmitter. The structure of the broadband PA is exhibited in Fig. 5. The PA includes a high-band PA, a low-band PA and two novel PD. The low-band PA uses off-chip matching network for obtaining optimal performance, while the high-band one uses an on-chip matching network to reduce the complexity of printed circuit board design. A cascode structure, which improves the break voltage and the output power, is applied into the broadband PA and the common-gate devices use the thick gate-oxide transistors. The sub-threshold PD is used to detect the output power. According to the voltage of the PD, the transmitter adjusts the bias of the common-source transistors in the proposed cascode structure so as to improve the PAE by the adaptive bias technique. The simulated PAE with and without the adaptive bias structure at 1 GHz is plotted in Fig. 6. The PAE is increased by the adaptive bias structure at the back-off mode.

3. Measured results and analysis

The proposed PA is manufactured at a TSMC 0.18µm technology process. The photo of the broadband PA is exhibited in Fig. 7. The die area of the broadband PA is 1.87mm² without the test pads.

The measured and simulated S-parameter results are demonstrated in Fig. 8. The S11 is lower than −11.46 dB and S22 is less than −7.87 dB from 45 MHz to 2500 MHz. The S21 varies from 12.23 dB to 13.95 dB. There is an error between the measured and simulated results, which are mainly caused by the effects on the parasitic parameters of the package and the printed circuit board. As exhibited in Fig. 9, the 1 dB output compression point (P1dB) of the proposed PA changes from 19.9 dBm to 21.3 dBm under single-tone signal measurement. The saturating output power (Psat) changes from 21.94 dBm to 24.02 dBm over a large frequency band. As plotted in Fig. 10, the maximum PAE achieves 44.61% at 500 MHz and the PAE is larger than 28.48% at 3 dB back-off mode over the whole frequency range. So the efficiency at the back-off mode of the proposed PA has been improved. Moreover, the meas-
ured error vector magnitude (EVM) with a 64 quadrature amplitude modulation (64QAM) signal centered at 1 GHz is plotted in Fig. 11.

The proposed PA is compared to the state-of-the-art broadband PA in Table I. The proposed PA with the sub-threshold PD, which provides higher PAE at back-off mode over a large frequency range compared with the other broadband PA, is a novel adaptive bias PA. The structure of the proposed PA, which uses the novel adaptive bias structure, is simple and the relative bandwidth is larger than the original adaptive bias technique.

4. Conclusions

This paper presents a method for decreasing the effect on frequency of adaptive bias technique. A novel adaptive bias is used as the common-source bias of the 45–2500 MHz CMOS PA, in which the scheme combines the subthreshold PD to decrease the effect on frequency of adaptive bias technique and a unity gain amplifier to increase the detection sensitivity. Meanwhile, the low output resistance of the unity gain amplifier is easy to drive the large filter capacitance and the large input resistance can improve the isolation of the sub-threshold PD. The fractional bandwidth of the broadband PA achieves 193% and the proposed PA provide a good performance from 45 MHz to 2500 MHz. The S21 changes from 12.23 dB to 13.95 dB. The P_{sat} varies from 21.94 dBm to 24.02 dBm with a 3.3 V supply and the PAE is larger than 28.48% at 3 dB back-off mode over the whole frequency range.

The proposed PA is compared to the state-of-the-art broadband PA in Table I. The proposed PA with the sub-threshold PD, which provides higher PAE at back-off mode over a large frequency range compared with the other broadband PA, is a novel adaptive bias PA. The structure of the proposed PA, which uses the novel adaptive bias structure, is simple and the relative bandwidth is larger than the original adaptive bias technique.

Table I. Result and comparison.

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<th>Ref</th>
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<td>15–20</td>
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References


