LETTER

A Ka-band 23 dBm power amplifier based on 4-way parallel-series power combiner with loaded capacitors in 65-nm CMOS

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Abstract This paper presents a Ka-band 4-way combining power amplifier (PA) implemented in 65 nm CMOS process. A T-type power combiner with loaded capacitors is proposed, which is cascaded with transformer-based power combiner to form a hybrid power combiner. The hybrid combiner can combine the output power of 4-way differential PAs into one channel compactly, and makes them achieve optimal load matching. The measured saturation output power (P_{sat}), output 1 dB compression point ($OP_{1\text{dB}}$) and maximum power added efficiency (PAE_{max}) are 23 dBm, 18.9 dBm and 27% at 35 GHz respectively. It achieves a 3 dB bandwidth of 30.7 GHz–38.5 GHz within a core area of 0.26 mm².

Keywords: CMOS, power amplifier, loaded capacitors, parallel-series hybrid power combiner, differential

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

In modern communication and radar system, the power amplifier (PA) is one of the core blocks in the transmitting channel, and its output power determines the overall output capacity and radiation distance of the system [1, 2, 3]. With the progress of technology, the research on silicon-based millimeter wave PA is becoming more and more popular. At present, the research of Ka-band PA is focused on the 5G millimeter wave communication system, which pays more attention to improving the back-off efficiency than to improving the output power of PA [4, 5, 6, 7]. However, in other applications, such as radar systems, it is more important to improve the saturation output power (P_{sat}) than the back-off efficiency.

Low resistivity of substrate, low breakdown voltage of transistor, serious parasitic effect and skin effect in millimeter wave band make it a challenge to realize high output power PA based on advanced CMOS technology [8, 9, 10, 11]. In recent years, varieties of researches focus on improving the output power by series or parallel power combining technique [12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23]. However, only depending on increasing the number of parallel or series PAs to improve the output power will lead to

high impedance conversion ratio (ICR), low efficiency and low gain. In Ref. [24, 25], the author changes the characteristic impedance of the transmission line by placing a floating metal bar at the bottom of the T-type power combiner, and then realizes impedance transformation and power combining. While, due to the limitation of process design rules, the range of changing characteristic impedance in this way is limited and discrete, and the effect is not obvious when dealing with the lower optimal load impedance.

In this paper, a T-type parallel power combiner (PPC) based on transmission line with loaded capacitors (TLLC) is proposed. By adjusting the position and value of the loaded capacitors, the characteristic impedance and phase velocity of the transmission line are changed. It is cascaded with transformer-based series power combiner (SPC) to form a parallel-series hybrid power combiner (PSHPC). Based on this, a high output power PA with 4-way differential power combining is proposed. The PA adopts a two-stage common source differential amplifier structure with neutralizing capacitors, which can improve the gain and stability. The proposed TLLC is described in section 2, the analysis and design of the proposed PA in detail is in section 3, and the measurement results are described in section 4.

2. A proposed transmission line with loaded capacitors

In the previous PSHPC, the T-type PPC is based on the two-wire transmission line with floating metal bars [24, 25]. The metal bars form a shield between RF signal line and substrate, which can reduce signal leakage [26]. At the same time, the characteristic impedance of the transmission line can be changed by adjusting the line width, spacing and layer, so as to realize the impedance transformation. However, the height and thickness of available metal layers and the dielectric are fixed in a specific CMOS process, and the width and spacing of metal wires are also limited by design rules. Generally, the range of characteristic impedance of transmission line changed in this way is limited and discrete.

The lossless equivalent model of the differential transmission line is shown in Fig. 1. The characteristic impedance Z_c and phase velocity v_p of the differential transmission line can be expressed as [27, 28]:

$$Z_c = \sqrt{\frac{2L(1-k)}{C_m + C_g/2}} \quad (1)$$

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Fig. 1 Equivalent model of differential transmission line

Fig. 2 Diagram of proposed TLLC

$$v_p = \frac{1}{\sqrt{2L(1-k)(C_m + C_g/2)}} \quad (2)$$

where, L is the series inductance of the transmission line, k is the coupling coefficient, C_m is the coupling capacitance between the two lines, and C_g is the coupling capacitance to the ground within a unit length.

According to Eq. (1) and (2), this paper proposes a transmission line structure with loaded capacitors in T-type PPC, as shown in Fig. 2. By adjusting the loaded capacitors, the Z_c of the transmission line is directly changed to complete the impedance transformation, and the v_p is reduced to form a slow wave structure so as to reduce the area.

Taking the transmission line shown in Fig. 2 as an example, the metal layer M9 is used as the signal transmission path, the line width w_1 and metal spacing s_1 are $10\mu\text{m}$, the length L_1 of the transmission line is $120\mu\text{m}$, and the loaded capacitors (C_c) are evenly arranged at the intervals of $10\mu\text{m}$ and $20\mu\text{m}$ respectively. Through electromagnetic simulation, Z_c and phase delay (θ_{delay}) versus C_c can be obtained at 35 GHz, as shown in Fig. 3. With the increase of loaded capacitance, the Z_c of the transmission line decreases and the θ_{delay} increases. The change of capacitors spacing is equivalent to the change of series inductance L of each equivalent unit in Fig. 1, which also affects Z_c and θ_{delay} . The simulation results verify the feasibility of adjusting Z_c and v_p of transmission line by adding loaded capacitance. By adjusting the metal line width and spacing, as well as the loaded capacitors value and spacing, the transmission line with desired Z_c and θ_{delay} can be obtained, and then a compact T-type power combiner can be formed.

3. Analysis and design of the proposed PA

3.1 PA configuration

The PA configuration proposed in this paper is shown in Fig. 4. The high output power PA is mainly composed of a two-stage amplifier structure, a PSHPC with loaded capacitors at the output, a T-type power division matching network at the input and an inter stage matching network. In order to improve the gain and stability, a common source differential topology with neutralizing capacitors is used in both stages. The output network of the power stage amplifier adopts the

Fig. 3 Simulated Z_c (a), and θ_{delay} (b) versus loaded capacitance

Fig. 4 Topology of the proposed PA with 4-way PSHPC

optimal load impedance matching to achieve higher output power. Conjugate matching is used in the inter-stage and input matching circuits to improve PA gain. The RF input and output ports are GSG single ended structure, and the internal structure of the proposed PA is differential to suppress common mode noise. The conversion between single ended and differential signal is completed by transformer-based balun.

Compared with [24], the major improvement of the proposed PA is to use the T-type PPC with loaded capacitors to complete the power combining and load impedance trans-

Fig. 5 Schematic and optimized layout of the common source differential amplifier with neutralizing capacitors

formation between load and transformers. It can better cope with the smaller optimal load impedance of large-scale output stage amplifier when it is co-designed with transformer-based SPC. The output of the power stage amplifier achieves optimal load matching compactly, and the whole PA achieves higher output power and efficiency.

3.2 Single stage amplifier with neutralizing capacitors

The proposed two-stage PA adopts a differential common source structure with cross-couple capacitors. By introducing a positive feedback capacitor C_N , the Miller effect is reduced, the power gain and stability are improved [29, 30]. Fig. 5 shows the schematic and optimized layout of one stage in the PA. The overall area of power stage amplifier is $25\ \mu\text{m} \times 90\ \mu\text{m}$ (including the surrounding ground ring). The two neutralizing capacitors are surrounded by the common source transistors on the left and right side. The input and output ports are located on the bottom and top sides respectively. Each side of the power stage is composed of four NMOSs ($4 \times \text{NM}_1$) with 32 fingers in parallel, and the gate length and width of single transistor are $60\ \text{nm}$ and $2\ \mu\text{m}$. Finally, the size of the driving stage is half of the power stage.

The power supply and bias voltage of the PA are $1\ \text{V}$ and $0.6\ \text{V}$ respectively. From the load pull simulation results, the ideal output $1\ \text{dB}$ compression point ($\text{OP}_{1\text{dB}}$) and P_{sat} are $15.2\ \text{dBm}$ and $18\ \text{dBm}$ under the optimal load of $Z_{\text{opt}} = 8.9 + j12\ \Omega$ at $35\ \text{GHz}$. Considering the losses caused by the output matching network and GSG pad, the actual $\text{OP}_{1\text{dB}}$ and P_{sat} are about $14\ \text{dBm}$ and $16.8\ \text{dBm}$. In order to achieve a P_{sat} of more than $22\ \text{dBm}$, it is necessary to use the 4-way power combiner.

3.3 Proposed 4-way parallel-series hybrid power combiner

The diagram of the proposed PSHPC is shown in Fig. 6. Firstly, the output power of the differential power stage amplifiers 1 and 2 (PA1 and PA2, as shown in Fig. 6) are combined by the transformer-based SPC to one channel. The output power of PA3 and PA4 are the same. Then, the 2-way output power are combined again by the T-type PPC with loaded capacitors. Therefore, the output power of the four power stages is combined into one channel and the output power is increased by $6\ \text{dBm}$.

The T-type PPC based on TLLC is shown in Fig. 7. The

Fig. 6 Diagram of the proposed PSHPC

Fig. 7 Layout of the proposed T-type PPC with loaded capacitors

Fig. 8 The 3D layout of transformer-based SPC

transmission line is mainly composed of M9, and the length, width and spacing of transmission lines are $130\ \mu\text{m}$, $12\ \mu\text{m}$ and $7.8\ \mu\text{m}$ respectively. 14 MOM capacitors (realized by M6 and M7) are used as loaded capacitors to adjust the Z_c and v_p . The center distance of the loaded capacitors is $19\ \mu\text{m}$ and the capacitance value is $8.2\ \text{fF}$. The bottom of the combiner is a integrity ground plane (composed of M1 and M2), which can be used to reduce signal leakage and avoid noise interference from the substrate.

The 3D layout and the top and bottom views of the transformer-based SPC used in this paper are shown in Fig. 8. The coils in the transformer are vertically placed for higher coupling coefficient and combining efficiency [13, 16, 24]. The primary coil of terminating PPC is mainly composed of M8, and the two secondary coils of terminating power stage amplifier are composed of M9. For the differential amplifier, the middle position of the two secondary coils can be used to feed the DC power supply, which is also regarded as AC virtual ground. Therefore, the power stage can be placed in the position of PA1 and PA2 in Fig. 8 respectively. In addition, it should be noted that the polarity of the other power stage amplifier need to be swapped.

As shown in Fig. 6, Fig. 7 and Fig. 8, Z_L represents the

Fig. 9 Optimal load matching through the proposed PCHPC

Fig. 10 Photograph of the proposed 4-way parallel-series combining PA

load, and Z_{L1} to Z_{L4} represent the load impedance at each node. The Z_L of 50Ω should be converted to the desired Z_{opt} ($8.9 + j12\Omega$) of PA1–4. It means that a large ICR matching network is necessary. For transformer, larger ICR means large insertion loss (IL), which is not conducive to improving the output power [13, 22, 24].

The impedance transformation trajectory of the PSHPC is shown in Fig. 9. Thanks to the proposed TLLC, the T-type PPC achieves a large ICR, therefore the ICR of SPC is reduced and the series combining efficiency is improved. The total IL of the hybrid combiner is about 1.5 dB, and the IL of the SPC and the PPC are 1.0 dB and 0.5 dB respectively. The hybrid combiner can achieve 4-way power combining and make each power stage amplifier matched to the optimal load.

4. Measurement results

The photograph of the proposed 4-way parallel-series combining PA is shown in Fig. 10, which is realized by low-cost 65 nm CMOS process within $520\mu\text{m} \times 500\mu\text{m}$ core area. The PA draws 660 mA current from a 1 V DC power supply in P_{sat} .

The S parameters of the proposed PA are measured with on-chip probe by vector network analyzer, and the comparison results between measured and simulation is shown in Fig. 11. It shows that the measured 3 dB bandwidth is 30.7 GHz–38.5 GHz, and the maximum power gain is 23.5 dB at 34.6 GHz. The output power and linearity of the PA are measured by signal generator and power meter. The measured output power, power gain and PAE versus input power at 35 GHz are shown in Fig. 12, respectively. It

Fig. 11 Comparison of measured and simulated S-parameters

Fig. 12 Measured output power, gain and PAE versus input power at 35 GHz

Fig. 13 Measured P_{sat} , OP_{1dB} and PAE_{max} versus frequency

depicts a P_{sat} of 23 dBm, a OP_{1dB} of 18.9 dBm and a PAE_{max} of 27%. Fig. 13 shows the P_{sat} , OP_{1dB} and PAE_{max} versus frequency within 3 dB gain bandwidth. The fluctuation of in-band P_{sat} and OP_{1dB} is less than 1 dBm. It shows that in-band P_{sat} is 22.2~23.16 dBm, OP_{1dB} is 18.2~19 dBm and PAE_{max} is 21.3%~27.4%.

The performance of the proposed 4-way combining PA is summarized in Table I [31, 32]. Compared with recently

Table I Performance summary and comparison with recently published Ka-band CMOS PAs

	[4]	[31]	[32]	[7]	This work
CMOS Tech.	28nm	28nm	90nm	65nm	65nm
Freq. (GHz)	30	34	34	28	35
V_{DD} (V)	1.15	0.9	1.2	2.4	1
Gain (dB)	16.3	20.8	19.8	15.9	23.5
P_{sat} (dBm)	15.3	16.6	20.7	23.2	23
OP_{1dB} (dBm)	14.3	13.4	18.5	22	18.9
PAE_{max} (%)	36.6	24.2	32.7	33.5	27
Area (mm ²)	0.16	0.16	0.2	0.25	0.26
Power density (mW/mm ²)	211.8	285.7	587.5	835.6	767.3
ITRS FOM	76.8	81.9	86.2	83.3	91.7

$$ITRS\ FOM = P_{sat} (dBm) + Gain (dB) + 20 \log(f_c (GHz)) + 10 \log(PAE_{max} (%))$$

published Ka-band CMOS process PAs, the proposed PA achieves good performance of gain, power density and ITRS figure of merit (FOM) in the table.

5. Conclusion

In this paper, a 65 nm CMOS Ka-band PA based on 4-way PSHPC is proposed. A TLLC is proposed, and then T-type PPC and load impedance converter are realized synchronously in a compact chip area. By cascading it with two transformer-based SPCs, the obtained PSHPC can combine the output power of 4-way differential power stage amplifiers into one channel, make each power stage amplifiers achieve optimal load matching. The measured results show that the 3 dB relative bandwidth of the PA is 30.7 GHz–38.5 GHz, the performance of P_{sat} and OP_{1dB} are 23 dBm and 18.9 dBm, and the PAE_{max} is 27%, the FOM is 91.7, all the performance above are at typical frequency.

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