LETTER

A 0.6V high-swing gate-switching charge pump for PLL with current self-matching technique in 28nm CMOS

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Abstract This letter presents a low voltage high-output-swing gate-switching charge pump (CP) used in phase-locked loops (PLL). The current self-matching technique is proposed to dynamically bias the gate of the current source transistors corresponding to output voltage fluctuation, keeping charging and discharging currents constant. To overcome the voltage margin issues under low supply voltage, a master-slave rail-to-rail operational trans-conductance amplifier (OTA) structure is proposed as the error amplifier of the negative feedback loop. The current mismatch of less than 2% is realized in the voltage range from 0.05 V to 0.55 V. A prototype of the proposed CP is designed and fabricated in TSMC 28nm CMOS process under a 0.6 V supply voltage. Charging and discharging currents are designed to be identical during the entire reset impulse. The measured reference spur is less than -59.4 dBc.

Keywords: charge pump, PLL, CMOS, self-matching technique

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

Supply voltage shrinkage is a prevalent approach in RF transceiver design for lowering the power consumption of portable wireless devices, in which a long charging cycle is a primary goal among all the performances [1, 2, 3, 4, 5, 6, 7, 8]. Furthermore, a lower supply voltage is inevitable due to breakdown issues in modern deep-submicron processes [9, 10]. Unfortunately, the threshold voltage is not much reduced in consideration of current leakage. This brings great difficulties to assign adequate voltage headroom for conventional analog circuits [9].

For a typical charge pump (CP) used in the frequency synthesizer, negative feedback loops are employed to guarantee the charging and discharging current matching [10, 11, 12]. Unfortunately, it can't work properly under low supply voltage below 0.7 V since numbers of stacked transistors are used inside of the operational trans-conductance amplifier (OTA) [13]. Some previous works use open-looped source switching structures as expedients [14, 15, 16]. However, it is inferior in current matching and reference spurs. Meanwhile, the voltage drop on the source

switches consumes a non-neglectable portion of the available output swing which is valued in low voltage design. For regular voltage designs, various techniques are proposed by previous works to improve the reference spurs [17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28]. However conventional techniques such as cascode and negative feedback can hardly work under low supply voltage because of the deficient voltage margin. To save voltage headroom for the CP's output swing, gate switching CP [29, 30] is a more promising solution than the source switching and drain switching structures, as shown in Fig. 1(a). The efficient output voltage range is between V_{DSATN} and $V_{DD} - V_{DSATP}$, which are the overdrive voltage of the charging and discharging transistors. However, the open-looped structure results in poor current matching and reference spurs. In this letter, a novel gate-switching CP with the current self-matching

(a) Conventional low voltage gate-switching charge pump

(b) Proposed self-matching gate-switching charge pump

Fig. 1 Circuit schematics of the gate-switching charge pump

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structure based on master-slave OTA is proposed. With gate-voltage dynamically compensated the current variation due to output voltage fluctuations, the charging and discharging current keep constant for a wide output range from 50 mV to $V_{DD} - 50$ mV. Simulation and measurement results also indicate less than 2% current mismatching and less than -59.4 dBc reference spur are realized.

2. Circuit design

The schematic of the proposed gate-switching CP is shown in Fig. 1(b). Charging and discharging currents are provided by P1 and N1 respectively, which are controlled by digital impulse signals CPP and CPN. The impulse generator is powered by 1 V V_{DD} to guarantee fast switching speed and low on-resistance. With error amplifiers A1 and A2 which are rail-to-rail master-slave OTA shown in Fig. 2, the current of P1 copies P2 and the current of N1 copies N2. A2 makes the drain terminal of the input reference current source equal to the core Vdd of 0.6 V, keeping the reference current constant. More importantly, A2 controls the gate of N1/2, making its current equal to the reference current all the time. A1 tracks the output voltage and dynamically changes the gate voltage of P1/2, compensating the current variation caused by the output voltage fluctuations. The charging and discharging current can be set constant even if N2 and P2 being forced into the triode region. Smoothing capacitor C1 and C2 are to provide charges for the charging and discharging switches, which helps to achieve steep on-edges in time-domain. In high-speed operation, the charging and discharging current are highly consistent under different output tuning voltage, which is the key for rejecting reference spurs. The branch of P2 and N2 is one of the output branches of the bandgap reference, which is powered by 1 V V_{DD} . With the output terminal of the reference branch being fixed to the 0.6 V core supply voltage, the currents of P2 and N2 are always constant.

A low voltage rail-to-rail OTA is also proposed in this letter to act as the error amplifiers in the CP, as shown in Fig. 2. Complementary gm stages are applied and their currents are superimposed by the common-gate stage. The master-slave structure compresses the V_{DS} of current tails, saving the voltage margin for input common-mode voltage and eliminating the dead zone near half of the supply voltage. Here taking the PMOS input stage to explain the principle of the master-slave structure, the first stage acts as a slave stage

Fig. 2 Schematic of the low voltage rail-to-rail master-slave OTA

that consists of the tail current transistor (M_3), the differential pair (M_{1a} and M_{1b}) and the current-mirror load (M_{11a} and M_{11b}). The master stage replicates the tail current source and the trans-conductance transistor of the slave stage, which means M_{2a} , M_{2b} and M_4 are the copies of M_{1a} , M_{1b} , and M_3 respectively. To save voltage margin, both M_3 and M_4 are biased in the near-linear region. The drain-source voltage of $M_{3/4}$ is defined as V_{DSL} , which is tens of mV. The minimum supply voltage, therefore, is $V_{TH} + 2 * V_{OV} + V_{DSL}$. The drain terminals of M_{2a} and M_{2b} are connected to the drain terminal of the current source M_5 and the gate of the M_4 , forming a negative feedback loop. When the input voltage of the OTA changes, the negative feedback loop automatically adjusts the gate voltage of M_5 to make its current equals the current source of M_7 . Since the master stage accurately replicates the slave circuit, the current flowing through M_3 remains constant.

Fig. 3 shows the simulated static charging and discharging current versus output voltage. For the conventional low voltage gate-switching structure, charging and discharging currents vary significantly with the output voltage due to the limited output impedance of P1&N1. For the proposed CP, the negative feedback tracks the output voltage and dynamically controls the gate voltage of P1&N1 to make charging and discharging current constant in almost the entire voltage range between V_{DD} and GND. The current mismatch is less than 2% in the voltage range from 0.05 V to 0.55 V.

In the PFD, a reset impulse of 0.5 nS width is designed to eliminate the dead-zone. During this phase, the charging and discharging currents must always be identical to avoid reference spurs. Fig. 4 shows the simulated charging and discharging current during the reset impulse of the proposed

Fig. 3 Simulated static charging (red) and discharging (blue) current versus output voltage of the proposed CP (solid lines) and the conventional switching-gate CP (dashed lines).

Fig. 4 Simulated charging (red) and discharging (blue) current during the reset impulse.

Fig. 5 Chip micro-photograph

Fig. 6 The output spectrum of the frequency synthesizer

CP. It is shown that the current curves almost coincide during the entire reset impulse.

3. Measurement results

Fig. 5 shows the micrograph of the proposed CP, which is part of a low voltage frequency synthesizer for BLE application in TSMC 28 nm CMOS process. The reference frequency is 24 MHz and the active area is $320\mu\text{m} \times 280\mu\text{m}$ including all of the decoupling capacitors. Fig. 6 shows the output spectrum of the frequency synthesizer. Thanks to the precise current matching, the reference spur of the frequency synthesizer is -59.4 dBc as indicated in the spectrum.

4. Conclusion

This letter presents a low voltage high-output-swing gate-switching CP with the current self-matching technique. To extend the output swing range under low supply voltage, a master-slave rail-to-rail operational trans-conductance amplifier (OTA) is employed to form the negative feedback loop. A prototype of the proposed CP is designed and fabricated in TSMC 28 nm CMOS process under a 0.6 V supply voltage. Charging and discharging currents are designed to be identical during the entire reset impulse. The measured reference spur is less than -59.4 dBc .

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