A 35-mV supply ring oscillator consisting of stacked body bias inverters for extremely low-voltage LSIs

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Abstract This paper proposes a ring oscillator (ROSC) for extremely low-voltage LSI applications. The ROSC consists of dedicated low-voltage stacked body bias inverters (SBBIs) that are based on the conventional self-bias inverter (SBI) and stacked inverter (SI). The proposed SIBI employs the advantages of both SBI and SI to oscillate at extremely low supply voltage. The voltage gain of the proposed SIBI is improved by controlling main inverter’s supply ($V_{T0}$ and Gnd) and body-bias voltages, by using stacked and feedback inverters. The novelty of our proposed SIBI is in the combination of the conventional low-voltage circuit design techniques and its demonstration at extremely low supply voltage. Simulated and measured results in a 0.18-μm CMOS process with deep n-well option demonstrated that the proposed ROSC can operate at extremely low supply voltage of 35 mV and generate a clock with an 88% voltage swing from an input supply voltage of 50 mV. To the best of the authors’ knowledge, this is the lowest supply voltage CMOS ring oscillator ever reported.

Keywords: startup oscillator, ring oscillator, inverter, power management, low-voltage energy harvesting

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

Energy harvesting techniques have attracted much attention as autonomous energy sources for next generation Internet of Things (IoT) applications [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11]. Thermoelectric generators (TEGs) can generate electric energy from a subtle temperature difference, and therefore they can be used as energy sources for wearable electronics applications. However, it is quite difficult to operate them stably because the output voltages of the TEGs are too low for LSI systems [12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24]. Therefore, a power management system (PMS) that can operate with an extremely low-voltage input is strongly required.

Figure 1 shows a block diagram of a fully on-chip PMS. The PMS consists of a DC-DC voltage boost converter and oscillator (OSC). The OSC generates a clock pulse from an input supply voltage $V_{IN}$ and is used to startup a DC-DC converter. However, when the input voltage becomes low, the OSC is not able to oscillate correctly because the voltage gain of the delay cells, or CMOS inverters, decreases as the supply voltage decreases.

Several low-voltage OSCs have been reported [25, 26, 27, 28, 29, 30]. Matsuzuka et al. reported a ring oscillator (ROSC) that can oscillate at a 42-mV supply voltage [27]. The ROSC uses self-bias inverters (SBIs) and the voltage gain of the SBI is enhanced by the body bias effect using an additional feedback inverter. Bose et al. developed an ROSC that can operate at a 40-mV supply voltage [28]. The ROSC uses stacked inverters (SIs) and the voltage gain of the SI is improved by the leakage current suppression technique using stacked inverters. As thus, low-voltage ROSCs have been intensively studied to realize extremely low-voltage energy harvesting systems.

In light of this background, we proposed an ROSC circuit capable of operating at extremely low supply voltage [30]. The proposed ROSC consists of dedicated low-voltage stacked body bias inverters (SBBIs) that are based on the conventional SBI and SI. The novelty of our proposed SBI is in the combination of the conventional low-voltage circuit design techniques and its demonstration at extremely low supply voltage. The proposed inverter employs the advantages of both SBI and SI to oscillate at extremely low supply voltage. In contrast to our previous work [30], here, we discuss its circuit operation and analyze its effectiveness in more detail. In addition, we fabricated a proof-of-concept chip in a 0.18-μm CMOS process to demonstrate the extremely low voltage performance of our ROSC.

This paper is organized as follows. Section 2 describes conventional inverters and presents our proposed inverter that can operate with extremely low supply voltage. Section 3 shows simulated and measured results, and Section 4 concludes the paper.

2. Inverters for extremely low-voltage ROSC

Figure 2(a) shows a schematic of the ROSC consisting of an
odd number of delay cells, or inverters. For oscillation to begin, the voltage gain of the inverter ($A_{INV}$) must be greater than unity.

$$|A_{INV}| \geq 1.$$  \hspace{1cm} (1)

However, the voltage gain $|A_{INV}|$ of the inverter decreases as the supply voltage decreases. Therefore, a CMOS inverter that has higher voltage gain is required. In the following, we briefly summarize conventional normal and high-gain inverters and explain our proposed inverter.

### 2.1 Conventional inverters

Figure 2(b) shows a schematic of the conventional normal inverter (NI). When current of nMOS transistor $I_N$ is equal to that of pMOS transistor $I_P$, the voltage gain of the inverter ($A_{INV}$) becomes maximum and can be calculated as

$$|A_{INV}| = \frac{1}{\eta} \left\{ \exp \left( \frac{V_{DD}}{2V_T} \right) - 1 \right\},$$  \hspace{1cm} (2)

where $\eta$ is the subthreshold slope factor and $V_T$ is the thermal voltage [27]. As shown in Eq. (2), the voltage gain decreases exponentially as $V_{DD}$ decreases.

As discussed in Sect. 1, in order to oscillate the ROSC at lower supply voltage, gain-enhanced CMOS inverters such as SBI and SI have been developed. Details of the inverters are described as follows.

Figure 2(c) shows a schematic of the SBI [27]. It consists of three inverters. The input voltage is applied to the body of the main inverter and controls threshold voltages $V_{TH}$ of the main inverter’s MOS transistors. The voltage gain of the SBI can be calculated as

$$|A_{INV}| = \frac{1}{\eta} \left\{ \exp \left( \frac{V_{DD}}{2V_T} \right) - 1 \right\} \left\{ 1 - \frac{1}{2} \frac{\partial(V_{TH})}{\partial V_{IN}} \right\},$$  \hspace{1cm} (3)

where $\partial(V_{TH})/\partial V_{IN}$ is the threshold voltage difference between nMOS and pMOS transistors in the main inverter. As shown in Eq. (3), the voltage gain of the SBI is improved because $\partial(V_{TH})/\partial V_{IN}$ becomes negative. The authors demonstrated that an ROSC consisting of the SBIs was able to oscillate at 42-mV power supply. Note that, as a similar body bias technique, the dynamic threshold-voltage MOS transistor (DTMOS) can also improve the voltage gain of the inverter [29]. However, as discussed in [27], the voltage gain of the SBI is superior to that of DTMOS.

### 2.2 Proposed inverter

As discussed above, the voltage gains of the conventional SBI and SI can be improved by the additional inverters. On the basis of these achievements, we propose a stacked body bias inverter (SBBI) by combining the merits of the SBI and SI. We consider that the voltage gain of the SBBI can be divided into two parts: the voltage gain of the SBI and the voltage gain of the SI. Figure 3 shows a schematic of two SBBIs connected in cascade. As shown in Fig. 3, we can find that the proposed SBBI has a higher voltage gain than the SBI and SI.

Figure 2(d) shows a schematic of the SI [28]. The SI consists of three inverters. The input voltage is applied to all inverters and the output voltages of inverter 1 and 2 are connected to the sources of the main inverter. Note that, normal and low $V_T$ transistors are used in the main and stacked inverters as shown in Fig. 2(d). As discussed in [28], the $|A_{INV}|$ of the NI can be expressed as

$$|A_{INV}| = \frac{g_{mN} + g_{mP}}{g_{dsN} + g_{dsP}}.$$

(4)

where $g_{mN}$ and $g_{mP}$ are transconductance, and $g_{dsN}$ and $g_{dsP}$ are the channel conductance at DC operating point, of nMOS and pMOS transistors, respectively. By using the additional stacked inverters (inverter 1 and 2), transconductances of nMOS and pMOS transistors in the main inverter increase, and thus the voltage gain of the SI increases compared with that of the NI. The $|A_{INV}|$ of the SI can be calculated as

$$|A_{INV}| = \frac{1 + |A_{INV1}| g_{mN} + (1 + |A_{INV2}|) g_{mP}}{g_{dsN} + g_{dsP}}.$$

(5)

where $|A_{INV1}|$ and $|A_{INV2}|$ are the voltage gain of inverters (inverter 1 and 2). The authors also demonstrated that an ROSC consisting of the SIs was able to oscillate at 40-mV power supply.
SBBI is based on the SBI and SI. In the same manner to the SI (Fig. 2(d)), normal and low $V_T$ transistors are used in the main and stacked inverters as shown in Fig. 3. In our proposed SBBI, the body bias voltage of the main inverter is controlled by the output voltage of the next stage inverter. This enables us to save a feedback inverter that is used in the SBI.

3. Simulation results

The performance of our proposed ROSC was evaluated by SPICE with a set of 0.18-μm CMOS process parameters. The number of SBBIs used in the ROSC was 27. The supply voltage $V_{DD}$ was set to 50 mV. For comparison, ROSCs using NIs, SBIs, and SIs, were also evaluated in the same technology and the number of each stages was set to 51, 31, and 39, respectively, to obtain almost the same frequency of 50 Hz. Note that, threshold voltages of normal and low $V_T$ transistors are about 500 mV and 350 mV, respectively.

Figure 4(a) shows the simulated voltage transfer curves (VTCs) of the inverters. The amplitudes of the NI, SBI, SI, and SBBI, were 38, 42, 44, and 46 mV, respectively. The output voltage of the SBBI changed steeply around the switching voltage. This means that the voltage gain of the SBBI was higher than those of the others. Figure 4(b) shows the simulated voltage gain, derived from Fig. 4(a). When $V_{IN} = V_{DD}/2 = 25$ mV, the voltage gains reached their maximum values. The maximum voltage gain of the SBBI was about 30,000 and it was 10,000 times higher than those of the others.

Figure 5 shows the simulated transient waveforms. The amplitudes of the ROSCs using NIs, SBIs, SIs, and SB-BIs, were 28.5, 39.2, 40.1, and 44.2 mV, respectively. Our proposed ROSC using SBBIs showed the highest voltage swing. In addition, simulated results also demonstrated that our proposed ROSC was able to oscillate at extremely low supply voltage, as low as 34 mV.

To investigate the circuit operation against process variation, we performed 1,000-run Monte Carlo statistical circuit simulations assuming die-to-die (D2D) global variations and within-die (WID) random mismatch variations in all MOS transistors using the parameters provided by the manufacturer. We compared the voltage swing of the ROSC using the SBIs, SIs, and proposed SBBIs. Figure 6 shows the simulated distribution. The proposed ROSC achieved the highest voltage swing among all the ROSCs.

4. Measurement results

We fabricated a proof-of-concept chip of our proposed ROSC using a 0.18-μm, 1-poly, 6-metal CMOS technology with deep n-well option. Figure 7 shows a chip micrograph of our proposed ROSC. The number of SBBIs was set to 27. For comparison, ROSCs using SBIs and SIs, were also fabricated in the same chip and the number of each stages was set to 31 and 39, respectively. In the measurement, we used source follower buffers to sufficiently drive off-chip parasitics. The bias current of the source follower buffer was set to 500 nA. The area of ROSCs using SBIs, SIs, and SBBIs occupied 0.015 mm$^2$, 0.034 mm$^2$, and 0.026 mm$^2$, respectively.

Figure 8 shows the measured waveform of ROSCs using
SBBIs at $V_{DD} = 50 \text{ mV}$. The voltage swing was 42 mV. The voltage swings of the ROSCs using SBIs and SIs were 35 and 37 mV (not shown in this figure). The highest amplitude was obtained by using our proposed SBBIs.

Figures 9, 10, and 11 show the measured supply voltage dependence of the ROSCs. Figure 9 shows the measured normalized amplitudes as a function of $V_{DD}$. Our proposed ROSC using SBBIs had the highest amplitude. In addition, the proposed ROSC could oscillate at extremely low supply voltage of 35 mV, while the conventional ROSCs (SBIs and SIs) at 40 mV. Figure 10 shows the measured frequency as a function of $V_{DD}$. The oscillation frequencies were almost the same dependence on the $V_{DD}$. The frequency of the proposed ROSC was slightly slower than that of the conventional ROSC. This was because our proposed SBBI uses both additional inverters and body bias technique, and the parasitic capacitance makes the frequency slow. Figure 11 shows the measured power consumption as a function of $V_{DD}$. The power consumption of ROSCs using SIs and SB-

<table>
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<th>$V_{DD}$ (mV)</th>
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<th>SI</th>
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BIs were higher than that of the ROSC using SBIs because they used two additional stacked inverters consisting of low $V_T$ transistors. The power consumption of our proposed ROSC was lower than that of ROSC using SIs. This was because the SBBI employed the self-biasing technique, which reduced the leakage current of the main inverter.

Figure 12 shows the measured minimum $V_{DD}$, or $V_{DD,\min}$, as a function of temperature. The ROSCs showed almost the same temperature dependence. The ROSC using the SBBIs achieved the lowest $V_{DD,\min}$. To investigate the $V_{DD,\min}$ of ROSCs in more detail, we performed further experiment. Table I shows the measured count of $V_{DD}$ where ROSCs were able to operate (10 samples in total). In all samples, the ROSCs using SBBIs was able to oscillate successfully as a function of $V_{DD}$ at samples at room temperature. Thus we defined the minimum $V_{DD}$ as 35 mV. The minimum $V_{DD}$ of the ROSCs using SBI and SI were 40 and 42 mV, respectively.

Figure 13 shows the measured (a) normalized amplitude,
In this paper, we proposed an ROSC for extremely low-voltage LSI applications. The proposed ROSC consists of gain-enhanced stacked body bias inverters (SBBIs). The voltage gain of the proposed inverter is improved by controlling main inverter’s supply (\(V_{DD}\) and Gnd) and body-bias voltages. Simulation and measurement results showed that the proposed SBBIs had higher amplitude and voltage gain, and can operate at the lowest voltage of 35 mV. The proposed ROSC is useful for extremely low-voltage energy harvesting systems.

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References


\[\begin{array}{|c|c|c|c|}
\hline
\text{Ref.} & \text{Inverter type} & \text{Tech.} & \text{Min. } V_{DD} \\
\hline
[25] & V_{TH}\text{-tuned} & 65 \text{ nm} & 15 & 82 \text{ mV} \\
\hline
[26] & \text{Selective schmitt-trigger} & 0.13 \mu \text{m} & 9 & 70 \text{ mV} \\
\hline
[27] & \text{SBI} & 0.18 \mu \text{m} & 31 & 42 \text{ mV} \\
\hline
[28] & \text{SI} & 0.18 \mu \text{m} & 21 & 40 \text{ mV} \\
\hline
\text{Prop.} & \text{SBBI} & 0.18 \mu \text{m} & 27 & 35 \text{ mV} \\
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Fig. 13 Measured (a) normalized amplitude, (b) frequency, and (c) power consumption, of our proposed ROSCs using SBBIs with temperature as a parameter.


