A novel power gating scheme with charge recycling

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Abstract: In MTCMOS, the circuit state should be preserved for state retentive sleep, and the virtual power/ground rails clamp (VRC) scheme is an effective method for this purpose. Our approach realizes the voltage clamp function without additional devices like diodes, by feeding the virtual ground voltage back into a sleep signal. There are also other effects; cutting off the leak current of the sleep buffer, and charge recycling of sleep signal node. We have achieved a 19.7% lower power consumption and a 5.4% cell area reduction.

Keywords: power gating, MTCMOS, low power, leak current, charge recycling, state retention

Classification: Integrated circuits

References

1 Introduction

Leak current has become one of the most important factors for low power design. The multi-threshold CMOS (MTCMOS) is an effective technique for leak current reduction [1]. This technique employs high $V_{th}$ MOS transistors to cut off the leak paths during sleep periods. However, MTCMOS loses the data in the circuit before sleep, since the leak current of the circuit charges the virtual ground to high level during sleep mode. The logical state in the circuit should be preserved during sleep mode to guarantee continuous circuit operation.

This paper proposes a new circuit scheme to preserve data during sleep the period for the power gating technique. We cut off the leak current of the sleep buffer and use charge recycling. Thus, we have achieved low power consumption in the sleep period with no additional clamp devices.

2 Virtual power/ground Rails Clamp (VRC) scheme

To preserve the circuit state during the sleep period, state retentive MTCMOS approaches have been proposed [2, 3]. These approaches write the state to external data storage before entering sleep mode. However, the data movement to external memory suffers from a power penalty, and thus they are unsuitable for short sleep periods.

The virtual power/ground rails clamp (VRC) [4] inserts diodes between virtual power/virtual ground (VGND) lines and real ones. In sleep mode, VGND is charged and the diodes clamp the voltage. Hence, the state can be preserved by limiting the rise of the virtual ground line voltage. Clark et al. [5] have also proposed a structure using a voltage comparator.

Kim et al. [6] have proposed a new VRC scheme with a pMOS transistor as the diode. They implemented state retentive and non-state retentive modes by controlling the pMOS diode input. Fig. 1 shows the circuit configuration and the voltage waveform of VGND. The waveform shows the behavior in which the circuit moves from active mode to state retentive sleep mode. In active mode, SLP and HLD are set to low and high, respectively. In sleep mode, SLP and HLD are set to high and low, respectively. Since the leak cut-off switch (MSW) cuts the current from VGND to GND, VGND rises passively. However, the VGND rise is limited by the threshold voltage of DP. Hence, the state is retained during sleep mode.

These VRC schemes perform power gating only for internal circuits. For low power design, we propose a novel power gating approach to reduce leak current through sleep control circuits as well as internal circuits.

3 Power Gating with Charge Recycling

Fig. 2 shows the proposed circuit configuration. We link the sleep signal node of the leak cut-off switch (NSW) and VGND by a sleep buffer nMOS (MBN). Since our approach does not use DP, we obtain the following advantages.
In active mode, SLP is set to low to turn on MSW, which makes VGND low. Then NSW is set to high and the electric charge is stored. In sleep mode, SLP is set to high and MBN conducts VGND and NSW. The charge stored at NSW flows into VGND through MBN. It charges VGND, and boosts the voltage. The conventional circuit abandons the electric charge stored at NSW to ground, and the leak current of the internal circuits raises the VGND voltage. We reuse the electric charge stored at NSW for boosting VGND. As a result, the current from VDD is reduced.

We have implemented the voltage clamp function of VGND by feeding the VGND back into NSW through MBN. As VGND is charged and the voltage rises near the threshold of MSW, it begins to turn on. Hence, the current from VDD is reduced.
Proposed circuit and the virtual ground waveform

Our approach links the source of MBN and GND through MSW. Hence, the sleep buffer is power gated. If the source node is charged to VDD voltage, NSW is set to high level and the circuit moves to active mode. However, VGND voltage of our approach is limited. Hence, we can keep a state retentive sleep mode and reduce the leak current from VDD to GND through MBN.

4 Implementation and Simulation Results

In this section we present the simulation results of the proposed and conventional approaches. We have implemented the proposed circuit and the conventional circuit [6] with 180 nm SOI technology. The supply voltage is 1.8 V. We have employed a benchmark circuit cm82a from the MCNC benchmark circuits. Fig. 3 shows the layout results by the proposed approach. The SPICE simulation temperature is 25 degrees. The threshold voltages with
MOSFETs are set to $V_{th,n} = 0.37 \text{ V}$, and $V_{th,p} = 0.35 \text{ V}$ for internal circuits and the sleep buffer, and $V_{th,n} = 0.42 \text{ V}$ for MSW, and $V_{th,p} = 0.35 \text{ V}$ for DP, respectively.

The conventional and proposed voltage waveforms of VGND are shown in Figs. 1 and 2. The circuits move from active mode to state retentive sleep mode. When moving to sleep mode, the VGND voltage of the conventional circuit becomes $-0.017 \text{ V}$ by the coupling capacitance between the gate and drain of MSW. The proposed circuit rises to $0.125 \text{ V}$ by the charge that is stored at NSW.

In sleep mode, the VGND voltage rises toward VDD by the leak current, and then the rate of increase slowly falls. The conventional VGND voltage rises to $0.266 \text{ V}$. The current through DP and the leak current of the internal circuits are balanced, and DP clamps VGND. The proposed approach works well, since we feed VGND voltage back into NSW.

Fig. 3 shows the leak current and cell area comparisons measure the leak current. As for the leak current, the conventional technique consumes $1.81 \text{ nA}$ at 50 us. The proposed circuit consumes $1.62 \text{ nA}$. We can reduce the leak current by 10.5% owing to the power gating of the sleep buffer. At 5 us, conventional circuit consumes $1.83 \text{ nA}$, and proposed one does $1.47 \text{ nA}$. The charge stored at NSW is reused. This charge recycling and power gating of the sleep buffer realizes a 19.7% lower power consumption.

As for the cell area, the proposed approach shows 5.4% smaller area than the conventional one, because no DP cell area is used.

<table>
<thead>
<tr>
<th></th>
<th>Leak Current [nA]</th>
<th>Cell Area [um$^2$]</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>5 [us]</td>
<td>50 [us]</td>
</tr>
<tr>
<td>Conventional</td>
<td>1.83</td>
<td>1.81</td>
</tr>
<tr>
<td>Proposed</td>
<td>1.47</td>
<td>1.62</td>
</tr>
<tr>
<td>Prop./Conv.</td>
<td>0.803</td>
<td>0.895</td>
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Fig. 3. Layout and Simulation Results
sleep control signal. Therefore, virtual ground is clamped without additional devices, such as diodes, and our approach reduces the cell area by 5.4%. The leak current is cut off for sleep buffers by linking the clamped virtual ground, and reduces the leak current by 10.5%. Our approach also employs charge recycling when circuits move to state retentive sleep mode, which leads to a 19.7% power consumption reduction. Our approach is applicable only to state retentive sleep. This is same as the original VRC schemes.

In particular, our approach is effective for short sleep periods, since there is a charge recycling structure for sleep control. Some SRAM circuits have VGND clamps and switch between clamp and non-clamp mode in a short time. The proposed approach will be applied to such circuits in future work.