G_m -boosted differential transimpedance amplifier architecture

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Abstract: A modified floating biased common-gate transimpedance amplifier with improved low corner frequency is introduced. It is also shown that g_m -boosting technique can be utilized for differential implementation of this transimpedance amplifier, without degrading the circuit sensitivity or using any off-chip components. HSPICE simulations for differential implementation illustrate more than two orders of magnitudes improvement of low corner frequency, about 80% increase in gain, and 20% reduction in input referred noise, compared to those of conventional single-ended floating biased common gate transimpedance amplifier.

Keywords: optical receiver, transimpedance amplifier, common gate configuration, floating biasing technique, g_m -boosting technique

Classification: Integrated circuits

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1 Introduction

In optical receivers, wideband transimpedance amplifier (TIA) is one of the most critical building blocks, as it is directly coupled to photodetectors (PD) to convert its current to an amplified voltage for data recovery. The need for high stability and low-power/low-voltage operation of TIA has resulted in designing common-gate (CG) and floating biased common-gate (FB-CG) configurations [1, 2]. However, differential implementation of TIA using conventional methods will degrade their noise performance or require extra cost such as using off-chip components [3].

In this letter, a modified FB-CG transimpedance amplifier (MFB-CGTIA) is presented which improves the low corner frequency by more than two orders of magnitudes compared to existing FB-CGTIA. In addition, g_m -boosting technique is utilized to implement the differential configurations for FB-CGTIA and MFB-CGTIA, without degrading the circuit sensitivity or using any off-chip components.

Section 2 gives a short review of FB-CGTIA. Section 3 presents the MFB-CGTIA. Section 4 introduces g_m -boosting technique for single-ended to differential conversion. Section 5 gives the simulation results. Finally, Section 6 concludes the paper.

2 Floating biased CGTIA

Fig. 1 (a) shows a conventional CGTIA, dc coupled to PD in order to have a wideband frequency response, extending from dc to high frequencies. However, the dc level fluctuation of photocurrent, i_{in} , due to changes in received optical power level, will affect the dc operating point of the circuit output, bringing many challenges in designing subsequent circuitry. A solution to this problem is providing a floating bias voltage using a floating current mirror for transistor M_1 , as shown in Fig. 1 (b) [1, 2]. In this way, the output dc voltage is kept constant despite variations in the PD dc current level.

3 Modified floating biased (MFB) CGTIA

In FB-CGTIA of Fig. 1 (b), the low corner frequency ω_L is:

$$\omega_L = \frac{1}{[1/g_{m0} + (1/g_{m1}) \parallel R_S]C_B} \approx \frac{g_{m0}}{C_B} \quad (1)$$

where g_{m0} and g_{m1} represent the transconductance of M_0 and M_1 , respectively. Note that $g_{m0} \ll g_{m1}$ since M_1 is n times larger than M_0 . This will also help reducing the power dissipation in M_0 .

In this section, we propose placing a resistance, R_B , in series with capacitor, C_B , to push ω_L to lower frequencies by few orders of magnitudes, as illustrated in Fig. 1 (c). In this figure, ω_L is:

Fig. 1. Common-gate configuration as TIA. (a) Conventional CGTIA. (b) Floating-biased CGTIA. (c) Modified floating-biased CGTIA. (b) Implementing R_B by series combination of pMOS and nMOS transistors.

$$\omega_L \approx \frac{1}{(R_B + 1/g_{m0})C_B} \quad (2)$$

As an efficient implementation, large R_B is realized using series pMOS and nMOS transistors as shown in Fig. 1 (d). In this case, the effective resistance of the series combination remains large [4] despite voltage fluctuation at the gates of M_0 and M_1 . However, for extremely large value resistors, coupling of signals through nonlinear parasitic capacitors of M_1 may results to an error voltage level on C_B . The gate-source parasitic capacitance, c_{gs} , has the main role in this process. Suppose c_{gs} is linear function of gate-source voltage of M_1 . Assuming that input current of PD has a sinusoidal form and $C_B \gg c_{gs}$, the value of error on C_B can be approximated as

$$V_{error} \approx \frac{1}{2} \frac{I_{in,max}^2 R_{in}^2 (\partial c_{gs} / \partial v_{gs})}{C_B} \quad (3)$$

In this equation, $I_{in,max}$ is maximum current swing of PD, R_{in} is input impedance of the TIA and $\partial c_{gs} / \partial v_{gs}$ shows the dependency of c_{gs} to variations in the gate-source voltage of M_1 . The error voltage, V_{error} , will dissipate through R_B during a period when the following is satisfied:

$$\frac{V_C}{R_B C_B f_{max}} \geq V_{error} \quad (4)$$

where V_C is the dc bias point of C_B , and f_{max} is the maximum available frequency of incoming signals. Thus, the possible value for R_B is:

$$R_B \leq \frac{2V_C}{I_{in,max}^2 R_{in}^2 f_{max} (\partial c_{gs} / \partial v_{gs})} \quad (5)$$

Note that the dominant pole of the TIA usually occurs at the input node due to high parasitic capacitance of the PD. Therefore, in this equation high corner 3 dB frequency of the TIA can be chosen as f_{max} .

4 Differential FB-CGTIA

In this section, we propose using g_m -boosting technique to implement the above single-ended FB-CGTIA and MFB-CGTIA with differential configuration. We will show that unlike the conventional method for single-ended to differential conversion; this technique will not degrade the circuit sensitivity or impose extra cost such as off-chip components to the system. Fig. 2(a) depicts the principle of g_m -boosting technique for a CG amplifier in which inverting amplification, A , is used between the source and gate terminals so that the effective transconductance of the transistor is increased by $(1 + A)$ [5]. A general realization of differential g_m -boosting technique is shown in Fig. 2(b) by capacitor cross coupling of two CG amplifiers [5] when the input is a differential signal. In Fig. 2(c) we have illustrated the possibility of using g_m -boosting technique for designing differential CGTIA where the single-ended input photocurrent, i_{in} , is directly sensed only by M_1 . Assuming that the cross coupling capacitors are sufficiently large compared to parasitic capacitances, $v_{gs1} = v_{gs2}$, where v_{gs1} and v_{gs2} represent the gate-source voltages of M_1 and M_2 , respectively. Therefore, neglecting the body effect and channel length modulation, $i_{d1} = i_{d2}$, where i_{d1} and i_{d2} denote the drain current of M_1 and M_2 , respectively. Thus, differential output signal is achieved, while differential transimpedance gain and output noise are doubled compared to that of single-ended one. As a result, the input-referred current noise will be reduced by a factor of $\sqrt{2}$, improving the circuit sensitivity by 3 dB. However, in practice, due to body effect as the main influencing factor $|i_{d2}| < |i_{d1}|$, and the improvement in transimpedance gain and noise characteristic may be lower. For instance, considering the body effect, and assuming $g_{m1} = g_{m2} = g_m$ and $g_{mb1} = g_{mb2} = g_{mb}$, the drain currents of M_1 and M_2 are:

$$\begin{cases} i_{d1} = g_m v_{gs1} - g_{mb} v_{s1} \\ i_{d2} = g_m v_{gs2} - g_{mb} v_{s2} = -g_m v_{gs1} - g_{mb} v_{s2} \end{cases} \quad (6)$$

where v_{s1} and v_{s2} represent the source voltage of M_1 and M_2 respectively. According to Eq. (6), the simplest way to achieve equal drain current values is to suppress the body effect of the transistors, i.e. $g_{mb} = 0$. However, this may be impossible due to technological limitations. An alternative method is setting the source resistance in M_2 , R_{S2} , to zero. In this case, $v_{s2} = v_{s1} = 0$

Fig. 2. Differential implementation of CGTIA. (a) Basic CG stage including g_m -boosting feedback amplifier. (b) Principle of differential g_m -boosting scheme realized by capacitor cross coupling of two CG stage. (c) Concept of single-ended to differential conversion by means of g_m -boosting technique. (d) Employing floating biasing technique in differential CGTIA. (e) Modified floating biased differential CGTIA.

where v_{g1} denotes the gate voltage of M_1 . Now Eq. (6) will change as follows.

$$\begin{cases} i_{d1} = -(g_m + g_{mb})v_{s1} \\ i_{d2} = g_m v_{s1} \end{cases} \quad (7)$$

Thus, neglecting the little difference between the drain currents due to body effect, eliminating R_{S2} approximately doubles the amplification gain in differential configuration.

Floating biasing in g_m -boosted differential CGTIA, as depicted in Fig. 2(d), enables dc coupling to PD. In this figure, the cross coupling capacitors will also play the role of gate capacitor C_B for floating biasing. Although floating biasing is needed only for M_1 , we use it for M_2 to match the characteristics of the two transistors.

Modified floating biasing as described above can further reduce the low corner frequency or provides the possibility of using smaller coupling capacitors, as shown in Fig. 2(e). Note that, in this figure R_{S2} is eliminated to increase the differential gain.

5 Simulation results

To evaluate the performance of the proposed schemes, the circuits in Fig. 1(b), (d) and Fig. 2(e) are simulated using a 0.13 μm CMOS process. A photodiode capacitance of 300 fF and a bondwire inductance of 500 pH are used for all simulations. The bias current is 50 μA and R_D is 200 Ω .

Fig. 3. Transimpedance gain vs. frequency for floating bi-ased CGTIA, modified floating biased CGTIA and new differential CGTIA.

Fig. 3 shows the frequency response of the circuits for $C_B=10$ pF. The upper 3 dB frequency of the circuits remain near 10 GHz, while the low corner frequency of 2.1 MHz for FB-CGTIA and less than 5 KHz for MFB-CGTIA is achieved. Transimpedance gain for differential CGTIA of Fig. 2(e) is 49.5 dB Ω (300 Ω) which is boosted by a factor of 1.82 compared to that of single-ended configuration in Figs. 1 (b) and (d).

HSPICE simulations indicate that compared to Figs. 1(b) and (d), our differential CGTIA topology of Fig. 2(e) has improved the circuit sensitivity by 1.8 dB that means the input referred current noise is reduced by a factor of 1.23, i.e., slightly less than $\sqrt{2}$. For a power supply of 1.2 V, the differential CGTIA consumes about 2.3 mW which is doubled compared to the circuits of Figs. 1 (b) and (d).

6 Conclusion

In comparison with conventional floating biasing technique in the design of transimpedance amplifiers, modified floating biasing scheme makes possible to use smaller gate capacitance for the same low corner frequency. Further, it is possible to utilize g_m -boosting technique for differential implementation of common gate transimpedance amplifiers, without degrading the circuit sensitivity or using any off-chip components.

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