An improved SRAM cell design for tolerating radiation-induced single-event effects

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Abstract: This paper presents an improved design of a radiation-hardened static random access memory (SRAM) cell. The memory cell is designed to be tolerant to transient single-event upsets by taking advantage of the fact that for the same area, the surface mobility of NMOS transistors is greater than that of PMOS transistors. The results show that the proposed design is able to withstand single-event upsets for temperatures between $-55^\circ C$ to $125^\circ C$ when subjected to radiation intensities of $10^{14}$ rad(Si)/sec without affecting the write performance of the memory. The circuit is also robust when impinging high energy particle strikes at various angles of incidence.

Keywords: Single-event upset, radiation-hardened SRAM

Classification: Science and engineering for electronics

References

1 Introduction

A single-event upset in a memory cell is caused when an ion strikes a $p$-$n$ junction. The ion may originate from cosmic rays, gamma rays, alpha particles, or protons and can strike the junction at varying angles of incidence. A node which is connected to a junction that is struck will track the charge movement as a voltage transient [1]. If this junction is connected to a data node within a cross-coupled bi-stable storage element of the memory cell, a soft error may occur. The commonly used six transistor SRAM memory cell is highly vulnerable to single-event upset and can cause the data stored in the cell to be lost. Researchers have designed radiation hardened SRAM cells by using cross-coupled gate resistors to guard against transient upsets [2, 3]. Modifications have been made to improve the performance of the resistively hardened memory cell [4, 5]. Although the hardening technique was able to prevent logic upset in the SRAM cell, the addition of the resistors resulted in performance degradation and was not suitable for certain applications. Further improvement was proposed in [6] by using six additional PMOS transistors. Fig. 1a shows the design of this radiation-hardened SRAM cell. The circuit has a better tolerance to single-event upset, but its recovery time compared to the original data was slow and increased the write time of the SRAM cell. This paper presents an improved radiation hardened memory cell design that is able to withstand higher intensities of single-event upset without compromising on the performance.

2 Proposed radiation-hardened memory cell design

Fig. 1b shows the proposed memory cell design. For the same chip area, NMOS transistors have a greater saturation current than PMOS transistors because of the differences in surface mobility. The saturation current for an NMOS device is three times the saturation current of a PMOS device, assuming that all other variables remain constant. The proposed SRAM cell design takes advantage of these inherent device characteristics. Nodes 4 and 5 store the data and the logic states are complementary. Nodes 7 and 8 off-load the memory cell during a read operation or during a write operation. Off-loading the memory cell avoids read/write speed degradation. To perform a write operation with a HI data bit, the data at node 1 is transferred to the data node 5 when the Wordline is pulsed logic HI. After the write operation is performed, nodes 5 and 8 are HI, while nodes 4 and 7 are LO. Also, control node 2 is LO and control node 9 is HI. To analyze the circuit response to a radiation strike, the vulnerable nodes are identified. In the proposed design, the vulnerable nodes are 4, 5, and 8. We study the behavior of these three nodes during a single-event upset and show how the effects are mitigated in the proposed improved design.

Case 1 - vulnerability of data node 4: Node 4 is critically vulnerable if the drain of the PMOS transistor P2 is struck. The excess charge will cause node 4 to go HI, causing a soft-error bit flip. To mitigate this, the HI state of node 8 in the proposed circuit keeps G3 turned ON, directing the excess charge to...
Fig. 1. (a) Radiation-hardened memory cell [6] (b) Proposed radiation-hardened memory cell

Case 2 - vulnerability of control node 8: Node 8 is vulnerable if the drain of the NMOS transistor G6 is struck, causing node 8 to potentially go LO. The removal of charge from node 8 causes transistor G3 to be incapable of keeping node 4 LO in the event that a successive strike perturbs data node 4 or 5. To circumvent this effect, the HI state of node 5 keeps transistor G4 in the ON state. In addition, the saturation current of G4 is greater than the saturation current of transistor G6. This enables rapid charge replacement on node 8 and restores it to the original HI state.

Case 3 - vulnerability of data node 5: Node 5 is critically vulnerable if the drain of the NMOS transistor N2 is struck. The excess charge will cause node 5 to go LO, causing a soft-error bit flip. If node 5 goes LO, the flip-flop action of the memory cell would try to drive node 4 to a HI state. To mitigate this, the HI state of the node 8 keeps G3 turned ON. Since G3 has been designed to have a greater saturation current than transistor P2, the voltage distribution in the P2-G3 conduction path keeps node 4 LO, making node 5 recover to the original HI state. Further analysis provides insights to the design of the proposed radiation hardened memory cell.

When a radiation strike occurs at the drain-substrate junction of transistor N2 connected to node 5, the induced photocurrent has an amplitude of $I_{hit}$ for a time duration of $t_p$. The area under the photocurrent versus time curve is equal to the charge removed from node 5. The charge will be $Q_{hit} = I_{hit} \times t_p$. Each node has a capacitance $C_i$, where $i$ denotes the node number. Assume that the change in node capacitance is negligible with respect to a change in the node voltage. The charge stored in node 5 is $Q_5 = C_5 \times V_5$. An ion strike generates a reverse current. The change in charge in node 5 takes place almost instantaneously with $Q_{5_{min}} = Q_5 - Q_{hit}$. The voltage at node 5 is given by $-V_{diode} \leq V_{5_{min}} \leq V_{DD}$, where $V_{5_{min}} = \frac{Q_{5_{min}}}{C_5}$. 

\[ Q_{hit} = I_{hit} \times t_p \]

\[ Q_{5_{min}} = Q_5 - Q_{hit} \]

\[ -V_{diode} \leq V_{5_{min}} \leq V_{DD} \]

\[ V_{5_{min}} = \frac{Q_{5_{min}}}{C_5} \]
Furthermore, for a worst-case condition assume that $Q_{hit} >> Q5$, causing the voltage at node 5 to fall to $V_{diode}$. This condition turns transistor N3 to the OFF state and turns transistor P2 to the ON state. To prevent a soft-error bit-flip, the circuit incorporates three characteristics. First, the voltage at node 8, $V8 = (V5 - V_{G4}) = (V_{DD} - V_{G4})$, turns transistor G3 to the ON state. Second, a voltage divider technique controls the voltage at node 4. During a radiation strike on node 5, the node 4 voltage must be low enough for P1 to stay in saturation. The technique utilizes the length (L) to width (W) ratios for resistance estimations of the ON devices. The present analysis uses transistors P2 and G3 for the ON devices. Transistor P2 is the pull-up device and transistor G3 is the pull-down device. If $Z_{pu} = L_{pu} / W_{pu}$ is the pull-up resistance ratio, $Z_{pd} = L_{pd} / W_{pd}$ is the pull-down resistance ratio, and $V_{tp1}$ is the threshold voltage of transistor P1, then the voltage at node 4 will be $V4 = Z_{pd} + Z_{pu} * V_{DD} \leq (V_{DD} + V_{tp1})$. It is known that PMOS devices suffer a threshold voltage shift, $V_{shift}$, up to a volt or more at post irradiation. Therefore, $V4 = \frac{Z_{pd}}{Z_{pu} + Z_{pd}} * V_{DD} \leq (V_{DD} + V_{tp1} + V_{shift})$. For this to occur, let $L_{pu} = L_{pd}$ and $W_{pd} \geq k W_{pu}$ where $k = \frac{V_{tp1} + V_{shift}}{V_{DD} + V_{tp1} + V_{shift}}$.

Third, the conditions on the channel width and channel length of the pull-up and pull-down devices affect the drain-to-source saturation currents of those devices. The saturation current is $I_{ds} = \frac{1}{2} \frac{\mu_{pu}}{L_{pu}} \left( \frac{W_{pu}}{2} \right) (V_{gs} - V_{th})^2$ for $0 < (V_{gs} - V_{th}) < V_{th}$. The major difference in the saturation currents of the pull-up and pull-down devices are surface mobility and the channel width of those devices, $\mu_{pd} > \mu_{pu}$ and $W_{pd} \geq k W_{pu}$. This implies that transistor G3 is capable of depleting more charge from node 4 than what transistor P2 is capable of supplying.

### 3 Performance of the proposed radiation-hard cell design

**Write cycle response:** The performance of the proposed memory cell is compared with previous designs. Since the write-time is longer than the read-time, only the write-time is analyzed. Initially, node 5 is in a LO state and node 4 is in a HI state. When $t = 1 \text{ ns}$, a HI state is written to node 5 and a LO state is written to node 4 and when $t = 5 \text{ ns}$, the single-event hit is simulated by subjecting node 5 to an 8 mA, 1 ns photocurrent pulse. The photocurrent generated when a particle strikes the p-n junction at 0° angle of incidence is given in Equ. (1) [7]. The circuit simulation uses Equ. (1) to generate the photocurrent equivalent to a single particle radiation with an intensity of $10^{14} \text{ rad(Si)/sec}$.

$$I_{pp}(t) = \Gamma g g A \left[ \left( W + L \text{ er} f \sqrt{\frac{t}{\tau}} \right) U(t) - \left( W + L \text{ er} f \sqrt{\frac{t - t_p}{\tau}} \right) U(t - t_p) \right]$$

(1)

where, $I_{pp}$ is the photocurrent in amps, $\Gamma$ is the dose rate in rads(Si)/sec, $g$ is the electron charge, $q$ is 4.2E13 carriers/(rad-cm²), $A$ is the junction area cm², $W$ is the depletion region width in cm, $L$ is the diffusion length in cm, $\tau$ is the minority carrier lifetime in sec, $t_p$ is the radiation pulse width in sec, $t$ is time in sec, and $U(t)$ is the unit step function of time.
Fig. 2. Write cycle response time when subjected to single radiation strike at $t = 5 \text{ ns}$ for a duration of 1 ns
(a) Regular unhardened memory (b) Resistively hardened memory (c) Radiation-hardened memory [6] (d) Proposed radiation-hardened memory

The response for the unhardened memory cell is plotted in Fig. 2a. The write time for this cell, which is about 1 ns, will be used as a reference. Clearly, the circuit does not withstand the ion strike, causing an upset in the data of the cell. Note that node 5 goes LO at $t = 5 \text{ ns}$ when the single-event upset occurs and does not recover to logic HI. The response for the resistively hardened memory cell is plotted in Fig. 2b. The normal write cycle for this cell is much longer, decreasing the speed of operation. Thus, the circuit conditions are invalid at the time of upset injection into node 5. The response to memory cell design described in [6] is shown in Fig. 2c. The write time for this cell is about 1.5 ns. However, a slight charge increase of 0.5 pC causes the memory cell operation to fail. To increase the single-event upset tolerance, the charge level for node 4 may be lowered by increasing the channel width of the hardening transistors. However, such an increase in width will increase the chip area used for transistor fabrication, causing the memory cell area to increase. The response for the proposed memory cell design is shown in Fig. 2d. Node 5 of the memory cell recovers to the HI state after the radiation strike. The write time is 1.5 ns which is comparable to 1 ns of the original memory cell. Also, note that node 4 remains in the LO state during the radiation strike.

Effect of varying operating temperatures: The performance of the proposed memory cell is subjected to various operating temperatures. The wide operating temperature range causes the critical charge to decrease as the temperature increases. The decrease in critical charge makes the circuit more vulnerable to single-event upset than under normal operating conditions. Results show that the proposed SRAM cell recovers from radiation strikes over the military temperature range of $-55^\circ \text{C}$ to $125^\circ \text{C}$. Figs. 3 a-d show that the response time of nodes 4, 5, 7 and 8 increases by 2.6 pS for every $^\circ \text{C}$ increase in temperature. This increase in response time is negligible compared to a regular write-time of the memory cell.

Effect of varying incidence angles of radiation strike: When a radiation par-
particle strikes a p-n junction at different angles of incidence, the photocurrent generated by an ion strike at any angle of incidence is given by \( I(t) = I_0 \sec(\theta) \left( e^{-\frac{t}{\alpha}} - e^{-\frac{t}{\beta}} \right) \) where, \( I_0 \) is approximately the maximum current at 0° angle of incidence, \( \theta \) is the angle of incidence, \( \alpha \) is the collection time constant of the junction, and \( \beta \) is the time constant of initially establishing the ion track [6]. Node 5 of the proposed memory cell was subjected to the photocurrents simulating radiation strikes at 0°, 45°, 88° on the p-n junction of transistor N2. Node 4 is initially 0 V and node 5 is at 5 V. After subjecting the cell to several radiation strikes, node 4 recovers to 0 V and node 5 recovers from radiation strikes at various angles of incidence. Even when a large photocurrent of magnitude 104 mA and time period 1 ns is applied, the response of node 5 in the proposed memory cell recovers to 5 V within 1.5 ns.

4 Conclusion

In this paper, an improved design of a SRAM cell is proposed. Circuit simulation results show that the cell is highly robust from the effects of radiation causing single-event upset. The memory cell is extremely tolerant to logic upset from impinging radiation particles having an intensity of 10^{14} \text{rad(si)/sec} at various angles of incidence and when subjected to a wide range of operating temperatures. The read/write-time of the cell is less than 2 ns, making it suitable for reliable high-performance applications.