A high performance low power 12-bit 40 MS/s pipelined ADC

Hua-Yu Jia\textsuperscript{a)}, Gui-Can Chen, and Hong Zhang
Department of Microelectronics, Xi'an Jiaotong University
Xianning Road 28, Xi'an, 710049, China
\textsuperscript{a}) jiahuyu@mail.xjtu.edu.cn

Abstract: A 1.8 V 12-bit 40 MS/s pipelined ADC fabricated in a 0.18 $\mu$m CMOS process is presented. The traditional closed-loop high performance residue amplifier in first stage is replaced by a simple open-loop amplifier to reduce power dissipation and increase circuit speed in the paper. To improve the stability and response speed of the amplifier, a novel circuit topology of open-loop amplifier is presented in this study. Also, a proposed (1+1)-bit/stage structure for pipelined ADC is used in the paper to convert residue voltage that exceeds the convert range. The occupied silicon area is $3.2 \times 3.7 \text{mm}^2$ and the power consumption equals 210 mW.

Keywords: pipelined analog-to-digital converter, residue amplifier, common-mode feedback

Classification: Integrated circuits

References


1 Introduction

Power dissipation is becoming an increasingly important design issue in pipelined analog-to-digital converter (ADC) for applications requiring battery operation. Most of the pipelined ADC’s power dissipation is caused by
residue amplifier circuits [1]. Thus, many recent papers study how to keep the power dissipation of residue amplifier low [2, 3].

In [1], the precision closed-loop residue amplifier is replaced by a simple power-efficient open-loop in the first stage of ADC. The nonlinearity error of open-loop amplifier is estimated and calibrated by a digital block. But in this design, the digital block for calibration and parameter estimation is implemented on an external field programmable gate array (FPGA). In addition, the open-loop amplifier still has complex structure and unstable stability.

This paper describes a 12-bit 40 MS/s pipelined ADC with a new open-loop amplifier topology fabricated in a 0.18 µm CMOS process. The new amplifier consumes less power dissipation because of its simple structure. The stability and response speed of the amplifier are all improved as common-mode feedback circuit is not needed. The paper also presents a new (1 + 1)-bit/stage structure in the second stage of the ADC to reduce convert error arise from residue voltage exceeds the convert range. In the design, the ADC block and digital calibration block are integrated in a same chip.

2 ADC architecture

The architecture is selected for the ADC because of its area and power saving capability. The block diagram of the ADC is shown in Fig. 1(a). The main parts of the ADC consists of an S/H stage, a 4-bit flash converter, an open-loop residue amplifier, a (1 + 1)-bit/stage stager and seven 1.5-bit stages followed by a 3-bit flash converter. The peripheral blocks include clock generator, a reference voltages generator and a bias current generator. The digital blocks consist of error correction and calibration circuits.

The supply voltage for the ADC is 1.8 V. Both the input and the internal differential signal swings are the same voltage (1.0 VPP).

3 Design of key building blocks

3.1 Open-loop residue amplifier

The open-loop residue amplifier that presents in [1] adopts a cascode architecture which can not operate with extremely small voltage supplies. To control common-mode feedback voltage, an extra circuit is needed. So, the power dissipation and area are relatively large.

A new open-loop residue amplifier topology is presented in the paper. As shown in Fig. 1(b), it contains a main amplifier and a gain control circuit. Simple differential pair architecture is chosen for lower power supply. The transconductance of the amplifiers’ input transistors is controlled by a replica amplifier and a differential difference amplifier (DDA).

The replica amplifier has a constant input with a value of \( V_{\text{ref}}/8 \). \( V_{\text{ref}} \) is a fixed reference voltage of the ADC. The output of the replica amplifier is given by:

\[
V_{\text{out}} = (V_{\text{rop}} - V_{\text{ron}}) \approx g_{\text{m5}} R_L (V_{\text{ref}}/8)
\]  

(1)

where \( g_{\text{m5}} \) is the transconductance of the input transistor \( M_5 \) in Fig. 1(b),

\[c\]
$R_L$ is the equivalent resistance of the resistors $R_4$, $R_5$, $R_6$.

The output voltage of replica amplifier is forced to equal the reference voltage $V_{\text{ref}}$ through negative feedback. We can express the output voltage of replica amplifier as

$$V_{\text{DDA}} = A_{\text{DDA}} (V_{\text{rop}} - V_{\text{ron}}) - V_{\text{ref}}$$  \hspace{1cm} (2)

where $A_{\text{DDA}}$ is the voltage gain of replica amplifier. Suppose $V_{\text{out}}$ increases $\Delta V$ arise from process or temperature. As a result, $V_{\text{DDA}}$ increases, thereby increasing the drain currents of $M_6$ and lowering the drain currents of $M_5$. Since $g_{m5} \propto I_{D5}$, $g_{m5}$ decreases and hence lower $V_{\text{DDA}}$.

The open-loop amplifier has a simple structure and the overall amplifier power dissipation is 5.5 mW. It’s reduced by 87% comparing with the amplifier in [1]. As common-mode control circuit is not needed, the stability and response speed of the amplifier are also improved.

### 3.2 (1 + 1)-bit/stage

The nonlinearity of the open-loop residue amplifier is calibrated by the signal
statistics-based digital calibration technique [1, 4]. The output codes of sub-ADC of the first sub-stage are modulated by a random sequence number. Therefore, there is no redundancy in the stage and gain offset will cause its residue to exceed the $\pm V_{ref}$ range. If the second stage still uses the 1.5-bit, in next stage, the convert error will occur and the output residue will exceed $\pm V_{ref}$ range.

To avoid this kind of convert error, this paper presents a new $(1 + 1)$-bit/stage structure for pipelined ADC by improving the 2-bit flash ADC. A system positive offset is added to the 2-bit flash ADC. That is, the decision levels of the comparators are increased by $0.25V_{ref}$ separately. To reduce the range of the output residue and obtain a symmetric curve, a $-0.75V_{ref}$ decision level is added. The changed residue curve is shown in Fig. 1 (c). The new curve shows that when the input signal is in $\pm 1.5V_{ref}$ range, the output residue remains within $\pm V_{ref}$ range. Therefore, the residue doesn’t exceed the input range of next stage. The residue transfer function shows that the structure has 3-bit output and 5 codes 000, 001, 010, 011, and 100. The resolution of the stage is $(\log_2 5) \approx 2.3$. To be distinguished with 1.5-bit and 2.5-bit, the structure is named $(1 + 1)$-bit/stage.

The circuit topology of the structure can be designed according to the residue function curve. The structure is shown in Fig. 1 (d). The sub-ADC that includes 4 comparators is used to quantize the analog input into 3-bit digital output. The multiplying DAC (MDAC) contains a DAC, a subtractor and an S/H amplifier. The output signal of the MDAC is

$$V_{res2} = 2 \times (V_{in2} - V_{DA2})$$

where 2 is the gain of the MDAC, $V_{in2}$ is the analog input signal and $V_{DA2}$ is the output signal of the DAC.

4 Measurements

The ADC is fabricated in a SMIC 0.18 $\mu$m CMOS process. All the data are measured at a supply voltage of 1.8 V and a sampling rate of 40 MHz. Power consumption of the ADC is 210 mW including all the power of the blocks shown in Fig. 1 (a) and the silicon area is 12.21 mm$^2$. In Fig. 2 (a) the die micrograph of the ADC is shown.

Figure 2 (b) and (c) shows the measured DNL and INL plots separately. The DNL is between $-0.3$LSB and 0.2LSB, and the INL is between $-0.4$LSB and 0.3LSB. Figure 2 (d) shows the measured output spectrum with an input signal frequency of 16.98 MHz. At this input signal, SFDR and SNDR equal 70.54 dB and 64.57 dB separately.

Table I shows a performance comparison between two similar products and this work. As can be seen from the table, the DNL and INL of this work are much higher than those of Ref. [5, 6]. The SINAD is higher than Ref. [6] but lower than Ref. [5]. Therefore, the static performance of this work has advantages and the dynamic performance should be improved in future work.
Fig. 2. (a) Die photograph; (b) DNL performance; (c) INL performance; (d) Measured output spectrum

Table I. Comparison with some previous works

<table>
<thead>
<tr>
<th></th>
<th>Resolution /bit</th>
<th>Conversion rate/MHz</th>
<th>Power /mW</th>
<th>SINAD /dB</th>
<th>DNL (max) /LSB</th>
<th>INL (max) /LSB</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work</td>
<td>12</td>
<td>40</td>
<td>210</td>
<td>64.54</td>
<td>0.3</td>
<td>0.4</td>
</tr>
<tr>
<td>Ref. [5]</td>
<td>12</td>
<td>65</td>
<td>300</td>
<td>70.2</td>
<td>0.4</td>
<td>Not available</td>
</tr>
<tr>
<td>Ref. [6]</td>
<td>12</td>
<td>40</td>
<td>188</td>
<td>63.5</td>
<td>0.5</td>
<td>2</td>
</tr>
</tbody>
</table>

5 Conclusion

A 12-bit 40 MS/s pipeline ADC operating at a supply voltage of 1.8 V is described. A new open-loop amplifier circuit and a (1 + 1)-bit structure are presented in the ADC to reduce power dissipation and converter error. Low power dissipation and high performance of static character have been obtained by using these new circuits.