

A novel approach to implement summing function for feedforward Δ - Σ AD modulator

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Abstract: A novel approach is proposed to implement summing function for feedforward Δ - Σ modulator. Unlike the conventional methods, neither summing op-amp nor a large number of summing capacitors are used in our design. The high-accuracy summing function is accomplished by using a few capacitors with small size to compensate the summing error caused by parasitic capacitance, thereby resulting in a smaller chip area and no additional power dissipation.

Keywords: summing function, feedforward, Δ - Σ modulator

Classification: Integrated circuits

References

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1 Introduction

High dynamic-range and wideband ADCs are endlessly desired to meet with the evolution of high performance system. However, with decrease of supply voltage and reduction of oversampling ratio (OSR), the performance degra-

distortion due to non-idealities of analog building blocks becomes serious for Δ - Σ modulator.

The full feedforward Δ - Σ topology with reduced sensitivity to integrator nonlinearities [1], makes it extremely suitable for low-voltage wideband applications. Compared to a feedback topology, the quantization noise transfer function (NTF) of feedforward topology remains the same, and the signal transfer function (STF) is unity, which is not affected by the non-idealities of analog building blocks. The internal signal swing can be well controlled by optimizing the loop coefficients, thus reducing modulator distortion significantly. Besides, only one feedback DAC needed remarkably simplifies the feedback circuit, especially for high-order design.

The feedforward Δ - Σ modulator as shown in Fig. 1 (a), however requires a summing function followed by a quantizer. Especially in multibit topology, this summing function cannot be simply realized by using the conventional switched-capacitor (SC) network shown in Fig. 1 (b). That is because, a coefficient α caused by parasitic capacitances C_P will induce error when comparing with various reference levels, as shown in Fig. 1 (c). This error coefficient can be represented as an α times amplifier after summing node in Fig. 1 (a), which may change the NTF of Δ - Σ modulator thereby reducing the effects of noise shaping.

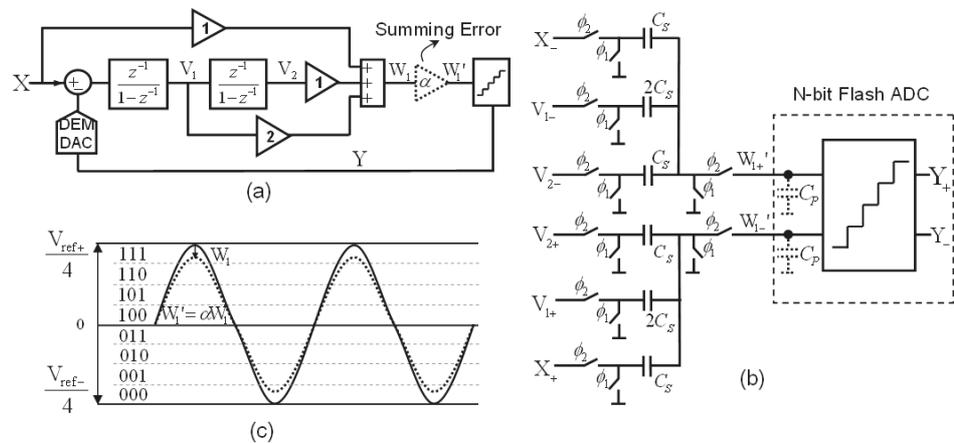


Fig. 1. (a) A second-order feedforward Δ - Σ AD modulator. (b) Conventional SC summing network. (c) Comparison mistakes in a 3-bit quantizer.

There have been reported several ways to implement the summing function. A method employing a SC summing op-amp to add the three feedforward signals induces a large output swing of the summing block. This method increases the ADC power consumption and presents stringent headroom requirements for summing op-amp [2]. Also, a large input swing demands more current consumption for quantizer, because the available input range of a differential pair is approximately proportional to I_{SS}/g_m . Another summing circuit using charge sharing is presented in [3]. By incorporating a capacitive network at each comparator input, the summing operation is accomplished

through charge sharing without any power penalty. This approach eliminates the need for a summing op-amp but demands a large number of capacitors, thus leading to a large extra chip area. For a second-order N -bit architecture, at least $6 \times (2^N - 1)$ units of capacitors are necessary.

Other methods such as digital summing technique [2] or by combining the summing function with the second-stage integrator [4] make design complex and are somehow affected by the limitations described above. In this work, we try to develop a simple but efficient way to implement the summing function with high accuracy. The proposed novel approach and the related calculations are demonstrated in Section II. Simulation results are presented in Section III and conclusions are drawn in Section IV.

2 Proposed summing circuit

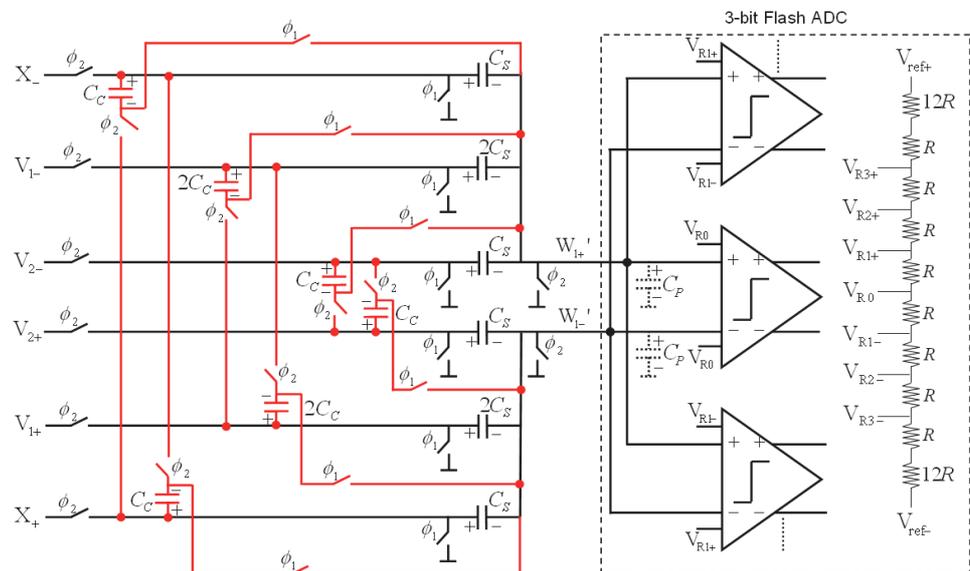


Fig. 2. The proposed summing circuit.

Figure 2 shows the proposed summing circuit for second-order feedforward modulator. It consists of a conventional SC charge sharing network followed by a multibit flash ADC, and compensation capacitor C_C routes denoted in red color. The differential signals X_+ , X_- , V_{1+} , V_{1-} , V_{2+} , V_{2-} and W'_{1+} , W'_{1-} represent the ADC inputs, two integrators outputs, and the summation results, corresponding to those shown in Fig. 1 (a). Capacitors C_S are used for the conventional SC charge sharing network. The parasitic capacitances C_P connected with input nodes of quantizer and switches causes a considerable degree of summing error because the value of C_P is usually above hundreds of femtofarad.

In order to improve the summing accuracy, compensation capacitors C_C are added to eliminate the summing error caused by C_P . The number of the compensation capacitors required in the proposed topology is independent of the quantizer bit numbers as far as their total value is equal to C_P . This

method can be extended to any order modulators just by increasing C_S and C_C SC routes according to the number of items in summation operation. Now, two kinds of conditions, without and with compensation capacitors C_C , are discussed to demonstrate the efficiency of our proposed topology.

2.1 Summing without compensation capacitors C_C

At end of clock phase ϕ_2 , the charge storage in capacitors C_S and C_P are:

$$\begin{aligned} Q_{C_{S\pm}} &= (X_{\pm} + 2V_{1\pm} + V_{2\pm})C_S \\ Q_{C_{P\pm}} &= 0. \end{aligned} \quad (1)$$

After changing to clock phase ϕ_1 , the differential summation voltage is:

$$\begin{aligned} \Delta W'_1 &= W'_{1+} - W'_{1-} = -\frac{(Q_{C_{S-}} - Q_{C_{S+}})}{4C_S + C_P} \\ &= \frac{4C_S}{4C_S + C_P} \frac{(X_+ - X_-) + 2(V_{1+} - V_{1-}) + (V_{2+} - V_{2-})}{4} \\ &= \alpha \times \frac{(\Delta X + 2\Delta V_1 + \Delta V_2)}{4} = \alpha \times \frac{\Delta W_1}{4}. \end{aligned} \quad (2)$$

ΔW_1 means ideal summation value, and α denotes the error coefficient, thus the summing error

$$\Delta\alpha_{calc.} = \alpha - 1 = -\frac{C_P}{4C_S + C_P} = -\frac{1}{4A + 1}, \quad (3)$$

where $A=C_S/C_P$. Eq. (3) suggests that a large C_S/C_P ratio is favorable for obtaining high-accuracy summing function.

2.2 Proposed summing using compensation capacitors C_C

At end of clock phase ϕ_2 , the stored charges in C_S , C_C and C_P are:

$$\begin{aligned} Q_{C_{S\pm}} &= (X_{\pm} + 2V_{1\pm} + V_{2\pm})C_S \\ Q_{C_{C\pm}} &= [(X_{\pm} + 2V_{1\pm} + V_{2\pm})C_C - (X_{\mp} + 2V_{1\mp} + V_{2\mp})]C_C \\ Q_{C_{P\pm}} &= 0. \end{aligned} \quad (4)$$

During phase ϕ_1 , the voltage levels at summing nodes:

$$\begin{aligned} W'_{1-} &= -\frac{Q_{C_{S+}} + Q_{C_{C+}} + Q_{C_{P+}}}{4C_S + 4C_C + C_P} \\ &= -\frac{(X_+ + 2V_{1+} + V_{2+})(C_S + C_C) - (X_- + 2V_{1-} + V_{2-})C_C}{4C_S + 4C_C + C_P} \\ W'_{1+} &= -\frac{Q_{C_{S-}} + Q_{C_{C-}} + Q_{C_{P-}}}{4C_S + 4C_C + C_P} \\ &= -\frac{(X_- + 2V_{1-} + V_{2-})(C_S + C_C) - (X_+ + 2V_{1+} + V_{2+})C_C}{4C_S + 4C_C + C_P}. \end{aligned}$$

Therefore, the differential summation voltage is:

$$\begin{aligned} \Delta W'_1 &= W'_{1+} - W'_{1-} \\ &= \frac{[(X_+ + 2V_{1+} + V_{2+}) - (X_- + 2V_{1-} + V_{2-})](C_S + 2C_C)}{4C_S + 4C_C + C_P} \\ &= \frac{4C_S + 4C_C + 4C_C}{4C_S + 4C_C + C_P} \times \frac{\Delta X + 2\Delta V_1 + \Delta V_2}{4} = \alpha \times \frac{\Delta W_1}{4} \end{aligned} \quad (5)$$

α denotes the error coefficient, so the summing error is represented by,

$$\Delta\alpha_{Calc.(Prop.)} = \alpha - 1 = \frac{4C_C - C_P}{4C_S + 4C_C + C_P} . \quad (6)$$

The summing error can be completely eliminated when using $4C_C=C_P$ although it is hard to realize in practical circuit design. The effect of capacitance mismatch on summation results can be evaluated by assuming $4C_C=\beta C_P$. The mismatch is shown as:

$$\Delta\beta = \beta - 1 = \frac{4C_C - C_P}{C_P} \quad (7)$$

Substituting Eq. (7) into Eq. (6), one obtains

$$\Delta\alpha_{Calc.(Prop.)} = \frac{\Delta\beta C_P}{4C_S + 2C_P + \Delta\beta C_P} = \frac{\Delta\beta}{4A + 2 + \Delta\beta} < \frac{\Delta\beta}{4A + 1} , \quad (8)$$

where A denotes C_S/C_P . The capacitance mismatch $\Delta\beta$ can be designed to be very small in general. Eq. (8) reveals that the summing error of the proposed topology is significantly reduced, approximately to $\Delta\beta$ times of that of the conventional one.

3 Simulation results

The proposed summing circuit are designed in $0.18\ \mu\text{m}$ CMOS process with $1.8\ \text{V}$ supply and MIM capacitors for C_S and C_C . Fully differential comparators are used for 3-bit quantizer. As shown in Fig. 2, a 4X attenuation occurs in comparator input, which is tolerable for Δ - Σ modulator. As discussed in Section I, this attenuated signal relaxes the requirement for comparator input range thereby decreasing power dissipation.

Simulations are run in two ways, without and with C_C routes. The differential DC signals X_+ X_- , V_{1+} V_{1-} and V_{2+} V_{2-} with a total amplitude of $1\ \text{V}$, are supplied to the input of summing circuits, then the summation results ΔW_1 ' can be obtained by simulations. In the first condition (without C_C), the simulation results and the calculation values derived by Eq. (3) are plotted in Fig. 3 (a). The figure shows that the C_S/C_P ratios of at least 5 and 25 are required in order to get summing errors of less than 5% and 1%, respectively. In Fig. 3 (a), the calculation values derived by Eq. (8) for proposed method are also shown for comparison. We can see that although for the large capacitance mismatch $\Delta\beta$ equal to $\pm 5\%$, $\pm 10\%$, $\pm 20\%$, the summing error are greatly reduced in comparison with the conventional one.

In simulation of the proposed method, it is important to estimate the value of parasitic capacitance C_P by Eq. (5), thus determining the optimum value of C_C by $C_C=C_P/4$, resulting $C_C=83\text{fF}$. By varying capacitance mismatch $\Delta\beta$ within $\pm 20\%$, the calculation and simulation summing errors are shown in Fig. 3 (b), with C_S/C_P ratio A equal to 1.5, 3 and 6, respectively. From the figure, we can see that a summing error of less than 1% can be easily achieved even at a small C_S/C_P ratio in comparison with the conventional one. Therefore, a significant reduction of total capacitance is achieved by the proposed method.

Since parasitic capacitance C_P changes with the variation of signal amplitude, in the proposed method, its effects on summation result are analyzed. The simulation results show that the summing error keeps variations within 0.2% over a signal swing of 1 V when $C_S/C_P=3$.

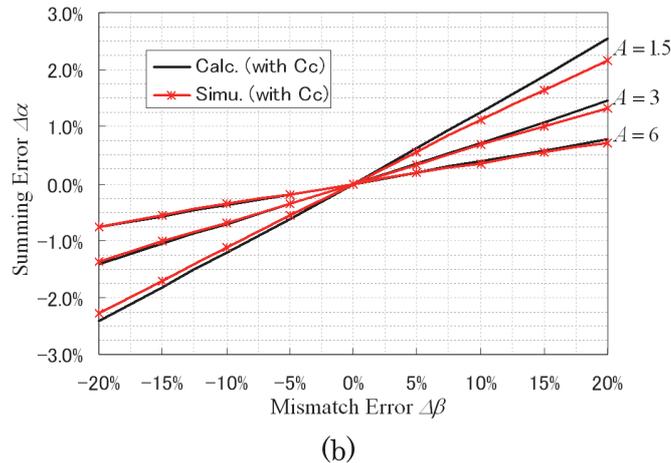
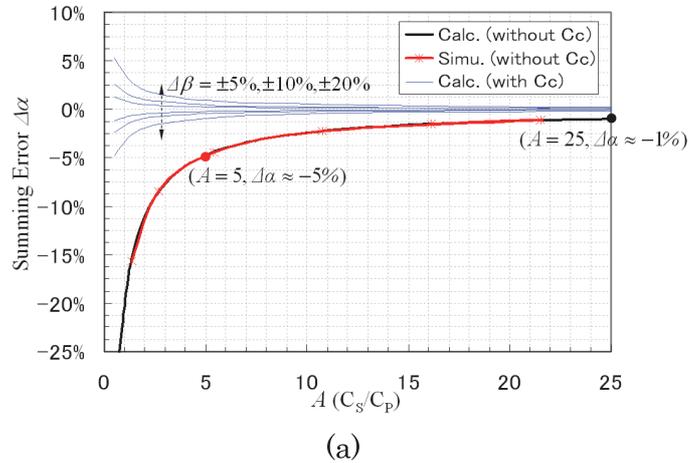


Fig. 3. Simulation and calculation results of summing circuits (a) without C_C (include the comparison with proposed methods), and (b) with C_C (proposed).

4 Conclusions

A novel approach to implement summing function for feedforward Δ - Σ modulator is proposed. By using small compensation capacitance, the summing error caused by parasitic capacitance in SC topology is substantially eliminated. Compared to the conventional methods, there is no additional power dissipation, and for a second-order N -bit modulator, the number of required capacitors are significantly decreased from $6 \times (2^N - 1)$ to 12, independent of bit number of quantizer. The proposed method increases design flexibility: a required summing accuracy can be realized by increasing sampling capacitance, or by adjusting the mismatch between compensation and parasitic capacitance. Therefore, op-amp load capacitance can be well controlled, which relaxes the requirements for integrator stages.

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