The design of high holding voltage SCR for whole-chip ESD protection

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Abstract: In this paper, we have investigated the electrical characteristics of Silicon Controlled Rectifier (SCR)-based ESD power clamp circuit with high holding voltage for whole-chip ESD protection. The proposed ESD power clamp circuit (HHVSCR: High Holding Voltage SCR) has different well (n/p-well) length (3/7 µm – 8/2 µm) and p-drift (p+) length (8 µm – 16 µm). The measurement results indicate that dimension of n/p-well and p-drift has a great effect on holding voltage (2 V–5 V) and a little effect on the triggering voltage (6.5 V–7 V). And the whole-chip ESD protection was designed for 2.5–3.3 V applications, this whole-chip ESD protection design can be discharged in ESD-stress mode (PD, ND, PS, NS) as well as VDD-VSS mode. The robustness of the novel ESD protection cells were measured to 6 kV (HBM: Human Body Model), 280 V (MM: Machine Model).

Keywords: ESD, SCR, triggering voltage, holding voltage

Classification: Electron devices

References

1 Introduction

Electrostatic Discharge (ESD) protection has become an important task on the reliability of CMOS IC’s. Silicon Controlled Rectifiers (SCRs) have long been as on-chip ESD protection elements over a board range of technologies because of their superior ESD protection behavior due to extremely high failure current and low on-resistance. But the advanced processes greatly degrade the ESD robustness of CMOS IC’s in the submicron CMOS technologies [1]. And when during ESD-stress conditions, the SCR must turn-on below sensitive voltages of the nodes to be protected within the circuit. And the device must not trigger during normal IC operation to ensure latch-up immunity (the SCR is used as a power) or signal integrity (SCR is applied as I/O protection). Thus the triggering voltage and holding voltage needs to be engineered. Also the stored ESD charges could be either positive or negative; there are four different ESD-testing modes at input-output (I/O) pins with respect to the grounded VDD or VSS pins [2]. Besides the four ESD-testing modes at I/O pins, two additional ESD-testing modes, pin-to-pin and the VDD-VSS ESD stresses, had been also specified to verify the whole-chip ESD robustness.

In this study, the High Holding Voltage SCR (HHVSCR)-based ESD clamp circuit was implemented to ensure latch-up immunity. And the whole-chip ESD protection design with high holding voltage is proposed for application in the 2.5-3.3 V (VDD) I/O circuit.

2 A Design of the ESD Power Clamp Circuit

ESD protection design using conventional devices (MOSFET, BJT, and diodes) is standard practice. However, even though the I-V characteristics of the conventional devices are more predictable and scalable to some considerations such as area efficiency, clamping voltage, on-state conductivity. The Silicon Controlled Rectifier (SCR)-type device is applicable for ESD protection because it exhibits snapback behavior and possesses a low holding voltage and a high conductance during an ESD event. However, the holding voltage of the SCR often causes the so-called latch-up problem in ICs [4]. Therefore the new structure of ESD protection circuit was designed for ESD power clamp circuit. The SCR-type, RC-based ESD protection device, so-called HHVSCR (High Holding Voltage-SCR) is shown in Fig. 1. This ESD protection circuit can provide effective ESD protection between VDD and VSS. This ESD clamp circuit is designed to be turned on when the ESD voltage appears across the VDD and VSS power lines.

In normal VDD power-on condition, PMOS is turn-off because the gate voltage of PMOS is not biased. N-well to P+ drift (the drain of PMOSFET) reverse blocking junction occur to avalanche breakdown at junction between N-well and P-drift because of the high electronic field. Then the ESD current through the QPDP flows into the P-well and P-drift region (drain of PMOS), and then forward biases the emitter-base junction of the QNPN turning it on. Also in the floating condition without power supplies, PMOS is turn-on.
because of the delay of R-C network and then forward biases the emitter-base junction of the Q\textsubscript{NPN} turning it on similarly.

So, this SCR-based power clamp has been operated with SCR operation (P\textsuperscript{++}-NW-PW-NW) in the floating condition and normal VDD power-on condition (because M\textsubscript{P} is kept off). So the internal circuits can be effectively protected without ESD damage in the power-on condition as well as the floating condition.

And the Q\textsubscript{NPN} current from the N-well to the cathode now supplies the forward-bias for the Q\textsubscript{PNP} and the voltage at the anode no longer needs to provide the bias for Q\textsubscript{PNP}. At this time, the holding voltage (V\textsubscript{H}) is written as Eq. (1) and is written as voltage drop between anode and cathode under conventional SCR’s high current conduction.

\begin{equation}
V_H = V_{BE}(Q_{PNP}) + V_{BE}(Q_{NPN})
\end{equation}

And each well current of proposed ESD power clamp circuit is written as Eq. (2) because the holding current relationship is the sum of base-emitter voltage of the pnp and npn transistor divided by the well resistance, respectively.

\begin{equation}
I_{NW} = \frac{(V_{BE})_{pnp}}{R_{NW}}, \quad I_{PW+P^+} = \frac{(V_{BE})_{npn}}{R_{PW}} + \frac{V_{P^+-drift}}{R_{P^+}}

(V_{P^+-drift} = V_{DD\,(anode)} - (V_{BE})_{pnp})
\end{equation}

At Eq. (2), I_{PW+P^+-drift} is the ESD current which is driven from anode and it passes through p-drift and P-well after avalanche breakdown. The V_{P^-drift} is voltage drop that extract base-emitter voltage of pnp transistor in voltage between V\textsubscript{DD} (anode) and V\textsubscript{SS} (cathode). And I_{P^+} is ESD current of P\textsuperscript{+-}drift region and is connected to V\textsubscript{SS} (cathode); I_{PW} is ESD current that flows from P\textsuperscript{+-}drift region to P-well in this ESD power clamp circuit. Only, the resistivities of N-well at cathode did not consider in this ESD power clamp circuit.
clamp.

\[(V_{BE})_{npn} = I_{(PW+P^+)} \times R_{PW} - \frac{(V_{P^+-drift} \times R_{PW})}{R_{P^+}}\]  

\[(V_{BE})_{npn} = \left[ I_{(PW+P^+)} - \frac{V_{P^+-drift}}{R_{P^+}} \right] \times R_{PW}\]  

From Eq. (1), the holding voltage is written as

\[V_H = (V_{BE})_{pnp} + \left[ I_{(PW+P^+)} - \frac{V_{P^+-drift}}{R_{P^+}} \right] \times R_{PW}\]  

The ESD protection circuit achieves electrical characteristic of the high holding voltage because the resistivities of the \(R_{P^+-drift}\) and \(R_{PW}\) (P-well) are dominant factor. Therefore the tuning of the holding voltage is readily accomplished by adjusting the dimensions ratio of N-well and P-well (D_1), the length of \(P^+-drift\) (D_2) from Eq. (5).

3 A Layout of Protection Cells for Whole-Chip ESD Protection

The layout is a critical step in the design and integration of the ESD protection structure in CMOS IC products. The ESD protection structure not only needs to be small and reliable, but also is required to fit in the space available and comply with all the design rules imposed by the IC-fabrication technology being used and the SoC development. Since the ESD stress may have positive or negative voltage on an I/O pins with floating VDD or VSS pins, there are four ESD-stress modes (PD, PS, ND, NS) on an I/O pins. Also there is discharge path (DS) between VDD and VSS owing to power clamp circuit in Fig. 2 [4]. Therefore the block diagram and layout design is proposed in Fig. 2 to design whole-chip ESD protection with four efficient ESD clamp between the VDD and VSS power lines for the whole-chip ESD protection scheme.

This design provide efficient discharge paths, pin-to-pin ESD stress and the VDD-to-VSS ESD stress, to achieve whole-chip ESD reliability. Also the designed ESD protection cells can reduce a number of pads (pins) and provides enhanced area efficiency because each input pad and output pad can be operated in four ESD-stress modes. And each ESD protection structures of the protection cell in ESD-stress modes are designed to multi-finger structure because the multi-finger structure has the advantages of robustness, and scalability is more immune to process variation [2]. The width of each ESD protection cell was designed to 60 um owing to 80 um of pad pitch. The dimension of the ESD protection cell including pad cell is 80 um × 160 um (L × W). Therefore because this ESD protection design with power clamp circuit can be discharged in ESD-stress mode (PD, PS, ND, NS) as well as VDD-VSS mode, This ESD protection scheme can provide enhanced area efficiency on the whole-chip.
Fig. 2. (a) The schematic diagram for whole-chip ESD protection (b) The layout of the whole-chip ESD protection design for the four ESD-stress mode (PD, ND, PS, NS) on an I/O pins and discharge between VDD and VSS power lines

4 Experimental Results

The proposed ESD clamp circuit was designed and fabricated in 130-nm CMOS process technologies. Fig. 3 (a) summarizes the values of $V_T$, $V_H$ with different internal lateral dimensions $D_1$, $D_2$ and the other dimensions in the device are kept at the minimum feature sizes allowed by the design rules.

In measurement results, Fig. 3 (a) shows that when the dimension of N-well is increased (3 um-8 um) and P-well is decreased (7 um-2 um) relatively, the holding voltage is decreased from 4.5 V to 3 V. And when the dimension of P-drift ($D_2$) is increased from 7 um to 16 um, the holding voltage is increased from 2.5 V to 5 V.

Therefore we could know that the holding voltage changes according to the dimension of P-well and P$^+$-drift in proposed power clamp circuit because the resistivities of P-well and P$^+$-drift are dominant as Eq. (5). Also the dimension of the protection cells were designed to 80 um $\times$ 80 um ($L \times W$) and the robustness of the novel ESD protection cells were measured to 6 kV (HBM), 280 V (MM) at worst case (NS mode) in Fig. 3 (b).
5 Conclusion

In this study, based on the RC time delay, an efficient SCR-based ESD power clamp circuit with high holding voltage was designed to ensure latch-up immaturity. The designed ESD protection circuit (HHVSCR) is adjusted by the dimension ratio of N-well and P-well (D1) and the dimension of P⁺-drift (D2) to increase holding voltage. In measurement results, the power clamp circuit (HHVSCR) is measured that when the dimension of N-well is increased and P-well is decreased relatively, the holding voltage is decreased from 4.5 V to 3 V. And the dimension of P⁺-drift (D2) is increased from 7 um to 16 um;
the holding voltage is increased from 2.5 V to 5 V. Also a whole-chip ESD protection design was established by using multi-fingers structure, the dimension of the ESD protection cell including pad cell is 80 μm × 160 μm (pad size: 80 μm × 80 μm). Finally, this ESD protection design with power clamp circuit can be discharged in ESD-stress mode (PD, PS, ND, NS) as well as VDD-VSS mode, the robustness of the novel ESD protection cells was measured to 6 kV (HBM), 280 V (MM). Therefore this ESD protection scheme can provide enhanced area efficiency, high latch-up immunity, high on-state conductance and high level of ESD models (HBM, MM) for 2.5~3.3 V VDD applications.

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