Experimental verification of the Chua’s circuit designed with UGCs

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Abstract: In this letter, experimental results of the Chua’s circuit designed with unity-gain cells (UGCs) are reported. The UGCs have been implemented with the commercially available integrated circuit (IC) AD844AN from Analog Devices. Parasitic elements of the UGCs are taken in account to design suitable the grounded inductor and the nonlinear resistor (NR) into Chua’s circuit. Experimental results are given, showing close agreement with theoretical conclusions.

Keywords: Chua’s circuit, unity-gain cells, double-scroll

Classification: Integrated circuits

References

[9] [online] http://www.analogdevices.org
1 Introduction

Chua’s circuit has been widely used for chaotic and nonlinear research [1, 2, 3, 4, 5, 6, 7, 8], since chaotic oscillators can be used in commercial applications such as medicine, biology and secure communications [7]. In the past design of chaos circuits, active devices such as: Current Feedback Operational Amplifier (CFOA) [4, 5], Operational Amplifier (OPAMP) [3], Operational Transconductance Amplifier (OTA) [2] and Second Generation Current Conveyor (CCII) [6] have been used as their building blocks. Recently, a new topology to design the Chua’s circuit which is based in UGCs, has been proposed and Hspice simulation results have been reported [8]. In this paper, we report experimental results of Chua’s circuit designed with this new topology as a sequel to [8].

2 Unity-Gain Cells Design

UGCs have become versatile analog building blocks in the analog signals processing, since they are recognized for its excellent performance in wider bandwidth, low bias voltage, low power consumption, simpler architecture compared with others more complex analog building blocks and high accuracy while operating in open-loop configurations, since their bandwidth is not inversely related to the closed loop gain [8]. For purposes of analysis, each UGC has been built with the IC AD844AN, since it is internally composed by two Voltage Followers (VFs) and one Positive Current Follower (CF+) [9].

Typical values of the parasitic elements connected to the terminals of the IC AD844AN are: $R_Y = 10 \, M\Omega$, $R_X = 50 \, \Omega$, $R_Z = 3 \, M\Omega$, $C_Y = 2 \, pF$, $C_Z = 4.5 \, pF$ [9]. According to IC AD844AN configuration, a VF can be built by connecting the X-terminal with W-terminal, as shown in Fig. 1 a. A CF+ is obtained by connecting the Y-terminal toward signal ground, as shown in Fig. 1 b. In order to obtain a CF-, two CF+ connected in cascade should be used, as shown in Fig. 1 c [8].

3 NR Architecture With UGCs

The topology of the NR with UGCs taken from [8] is shown in Fig. 2 a. Here, parasitic elements associated to the terminals of the IC AD844AN are taken in account, therefore, it can easily be shown that the node voltages $V_X$ and $V_Y$ in Fig. 2 a can be approximated as:

$$V_X \approx V_N \left(1 + \frac{Z_2 Z_{22}}{Z_1 (Z_{22} + Z_{X3})}\right)$$

$$V_Y \approx V_N \left(1 + \frac{Z_4 Z_{44}}{Z_3 (Z_{44} + Z_{X5})}\right)$$

The currents flowing through $Z_2$ and $Z_4$ are given as:

$$i_{Z_2} = \frac{1}{Z_2} (V_N - V_X), \quad i_{Z_4} = \frac{1}{Z_4} (V_N - V_Y)$$
The input currents to both CF’s are provided by \( V \), and following the same analysis as in [8], the new breakpoints and linearly with the input (linear region). This way, by considering parasitic elements and when the input current is small in magnitude, the output varies almost constant at \( E^{+}\text{sat} \) (positive saturation region), the maximum negative output voltage is \( E^{-}\text{sat} \) (negative saturation region) and when the input current is small in magnitude, the output varies almost linearly with the input (linear region). This way, by considering parasitic elements and following the same analysis as in [8], the new breakpoints and slopes of the NR are modified as:

\[
\begin{align*}
  m_0 &= \frac{1}{Z_2} + \frac{1}{Z_3} \\
  m_1 &= \frac{1}{Z_2} + \frac{Z_1(Z_2+Z_3)[Z_2(Z_2+Z_3)]}{Z_4Z_5} \\
  m_2 &= \frac{Z_1(Z_2+Z_3)Z_2(Z_2+Z_3)}{Z_1(Z_2+Z_3) + Z_3(Z_2+Z_3)} \\
  \pm E_1 &= \pm \frac{E^{+}\text{sat}}{1 + \frac{E^{+}\text{sat}}{Z_2Z_3}} \\
  \pm E_2 &= \pm \frac{E^{+}\text{sat}}{1 + \frac{E^{+}\text{sat}}{Z_2Z_3}} \\
  \pm E_3 &= \pm E^{+}\text{sat}
\end{align*}
\]

4 Active Grounded Inductor Architecture

The design of the active grounded inductor by using UGCs, is depicted in Fig. 2 b. Again, by considering parasitic elements and following the analysis...
If the parasitic elements are insignificant, then the Eq. (8) is reduced to [8]:

\[
\frac{V_{IN}}{I_{IN}} \approx sC_{B}R_{1}R_{2} = sL_{eq}
\]

5 Chua’s Circuit Architecture and Experimental Results

The Chua’s chaotic oscillator circuit implemented with UGCs, is shown in Fig. 2c. This circuit was also implemented in the laboratory using the IC AD844AN from Analog Devices with ±5 V voltage supply. For purposes of experimentation, we have fixed the following values of the elements: \(R_{1} = 1.8 \, k\Omega, R_{2} = 560 \, \Omega, R_{3} = 2.2 \, k\Omega, R_{4} = 4.7 \, k\Omega, R_{5} = 560 \, \Omega, R_{6} = 18 \, \Omega, R = 1.5 \, k\Omega, C_{1} = 22 \, nF, C_{2} = 1 \, uF\) and \(C = 470 \, nF\). The inductor is approximated to \(L = 4.7376 \, mH\), where the parasitic resistances and capacitances of the VFs and CFs have been considered. The inductor along with the NR, both designed with UGCs show a good behavior at low frequency. We note that the parasitic resistors associated to the input terminal of a CF
and at the output terminal of a VF play an important role in the inductor behavior and of the NR, since they impose a low-limit on the values of $R_1$, $R_3$, $R_5$ and $R_6$. Furthermore, one should have care also with the parasitic capacitances, since the discrete capacitors should be large enough to minimize the effect of the parasitic capacitor at nodes Y and Z of the IC AD844AN. On the other hand, the double scroll attractor measured in the laboratory is shown in Fig. 3a. A good agreement of the theoretical analysis [8] with the experimental results is evident. Finally, the chaotic waveforms in the time domain are shown in Fig. 3b.

6 Conclusions

We have demonstrated experimentally that the Chua’s chaotic circuit can be designed with UGCs. In this case, each UGC has been implemented in the laboratory by using the IC AD844AN and a consequence, the NR and the grounded active inductor can easily be built. Likewise, the equations that model the behavior of the slopes and breakpoints associated to the NR as well as of the grounded active inductor, have been deduced. Experimental results in the time domain and in the state space have been shown for illustrating the capability of the proposed topology.

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