Physical design challenges to nano-CMOS circuits

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Abstract: There are many challenges inherent in the design of nano-CMOS. This paper describes our recent work relating to the physical design of CMOS circuits. First, in line with variation-aware design, a novel ingenious method of measuring variations in subthreshold characteristics is described. Next, recent RF CMOS issues and approaches to nano-CMOS are discussed. Finally, an on-chip transmission line interconnect developed for global wiring is discussed.

Keywords: CMOS, scaling, RF CMOS, interconnect integration, integration of diverse functionalities

Classification: Integrated circuits

References

- [1] R. H. Dennard, F. H. Gaensslen, V. L. Rideout, E. Bassous, and A. R. LeBlanc, “Design of ion-implanted MOSFETs with very small physical dimensions,” *IEEE J. Solid-State Circuits*, vol. SC-9, no. 5, pp. 256–268, Oct. 1974.
- [2] T. Ohmi, “ULSI reliability through ultraclean processing,” *Proc. IEEE, Special Issue on VLSI Reliability*, vol. 81, no. 5, pp. 716–729, May 1993.
- [3] M. Aoki, S. Ohkawa, and H. Masuda, “Design guidelines and process quality improvement for treatment of device variations in an LSI chip,” *IEICE Trans. Electron.*, vol. E88-C, no. 5, pp. 788–795, May 2005.
- [4] K. Takeuchi, T. Fukai, T. Tsunomura, A. T. Putra, A. Nishida, S. Kamohara, and T. Hiramoto, “Understanding random threshold voltage fluctuation by comparing multiple fabs and technologies,” *IEEE International Electron Devices Meeting (IEDM)*, pp. 467–470, Dec. 2007.
- [5] T. Sato, H. Ueyama, N. Nakayama, and K. Masu, “A MOS transistor array with pico-ampere order precision for accurate characterization of leakage current variation,” *IEEE Asian Solid-State Circuit Conference (ASSCC)*, pp. 389–392, Nov. 2008.
- [6] M. Imai, T. Sato, N. Nakayama, and K. Masu, “An evaluation method for the number of Monte Carlo STA trials,” *IEICE Trans. Fundamentals*, vol. E91-A, no. 4, pp. 957–964, April 2008.
- [7] M. Imai, T. Sato, N. Nakayama, and K. Masu, “Non-parametric statistical static timing analysis: An SSTA framework for arbitrary distribu-

- tion,” *45th Design Automation Conference (DAC)*, pp. 698–701, June 2008.
- [8] A. A. Abidi, “Direct-conversion radio transceivers for digital communications,” *IEEE J. Solid-State Circuits*, vol. 30, no. 12, pp. 1399–1410, Dec. 1995.
- [9] K. Okada, Y. Yoshihara, H. Sugawara, and K. Masu, “Design of Reconfigurable RF CMOS Wireless Circuit,” *IEICE Trans. Electron.*, vol. J89-C, no. 7, pp. 499–507, June 2006 (in Japanese).
- [10] K. Masu and K. Okada, “Reconfigurable RF CMOS circuit for cognitive radio,” (Invited Paper), *IEICE Trans. Commun.*, vol. E91-B, no. 1, pp. 10–13, Jan. 2008.
- [11] K. Okada, H. Sugawara, H. Ito, K. Itoi, M. Sato, H. Abe, T. Ito, and K. Masu, “On-chip high-Q variable inductor using wafer-level chip-scale package technology,” *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2401–2406, Sept. 2006.
- [12] Y. Ito, H. Sugawara, K. Okada, and K. Masu, “A 0.98 to 6.6 GHz tunable wideband VCO in a 180 nm CMOS technology for reconfigurable radio transceiver,” *IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pp. 359–362, Nov. 2006.
- [13] Y. Kobayashi, K. Ohashi, Y. Ito, H. Ito, K. Okada, and K. Masu, “A 0.49–6.50 GHz wideband LC-VCO with high-IRR in a 180 nm CMOS technology,” *Int. Conf. Solid State Devices and Materials (SSDM)*, Tukuba, pp. 268–269, Sept. 2007.
- [14] K. Masu, K. Okada, and H. Ito, “RF passive components using metal line on Si CMOS,” (invited paper), *IEICE Trans. Electron.*, vol. E89-C, no. 6, pp. 681–691, June 2006.
- [15] D. Linten, X. Sun, G. Carchon, W. Jeamsaksiri, A. Mercha, J. Ramos, S. Jenei, P. Wambacq, M. Dehan, L. Aspemyr, A. J. Scholten, S. Decoutere, S. Donnay, and W. D. Raedt, “Low-power voltage-controlled oscillators in 90-nm CMOS using high-quality thin-film postprocessed inductors,” *IEEE J. Solid-State Circuits*, vol. 40, no. 9, pp. 1922–1931, Sept. 2005.
- [16] K. Kuwabara, N. Sato, H. Morimura, J. Kodate, M. Nakamura, M. Ugajin, T. Kamei, K. Kudou, K. Machida, and H. Ishii, “Integrated MEMS LC resonator with sealed air-suspended structure for single-chip RF LSIs,” *IEEE Int. Electron Device Meeting*, pp. 423–426, Dec. 2007.
- [17] K. Itoi, M. Sato, H. Abe, H. Sugawara, H. Ito, K. Okada, K. Masu, and T. Ito, “On-chip high-Q Cu inductors embedded in wafer-level chip-scale package for silicon RF application,” *Proc. IEEE MTT-S Int. Microw. Symp.*, pp. 197–200, June 2004.
- [18] H. Hatakeyama, Y. Uemichi, K. Ohashi, S. Fukuda, H. Ito, K. Okada, T. Aizawa, T. Ito, and K. Masu, “RF CMOS circuits with wafer-level packaging inductors,” *Int. Wafer-Level Packaging Conf.*, pp. 69–73, Oct. 2008.
- [19] K. Ohashi, Y. Kobayashi, H. Ito, K. Okada, H. Hatakeyama, T. Aizawa, T. Ito, R. Yamauchi, and K. Masu, “A low phase noise LC-VCO with a high-Q inductor fabricated by wafer level package technology,” *Radio Frequency Integrated Circuits Symposium 2008 (RFIC 2008)*, pp. 123–126, June 2008.
- [20] A. Matsuzawa, “Mixed Signal SoC Era,” *IEICE Trans. Electron.*, vol. E87-C, no. 6, pp. 867–877, June 2004.
- [21] C. Nguyen, “MEMS technology for timing and frequency control,” *IEEE Trans. Ultrason. Ferroelectr., Freq. Control*, vol. 54, no. 2, pp. 251–270, Feb. 2007.
- [22] R. B. Staszewski, K. Muhammad, D. Leipold, C.-M. Hung, Y.-C. Ho,

- J. L. Wallberg, C. Fernando, K. Maggio, R. Staszewski, T. Jung, J. Koh, S. John, I. Y. Deng, V. Sarda, O. Moreira-Tamayo, V. Mayega, R. Katz, O. Friedman, O. E. Eliezer, E. de Obaldia, and P. T. Balsara, “ALL-Digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130 nm CMOS,” *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2278–2291, Dec. 2004.
- [23] R. B. Staszewski, J. Wallberg, S. Rezek, C. M. Hung, O. Eliezer, S. Vemulapalli, C. Fernando, K. Maggio, R. Staszewski, N. Barton, M. C. Lee, P. Cruise, M. Entezari, K. Muhammad, and D. Leipold, “ALL-Digital PLL and GSM/EDGE transmitter in 90 nm CMOS,” *IEEE Int. Solid-State Circuits Conf.*, pp. 316–317, Feb. 2005.
- [24] H. Kobayashi, “Analog circuit design in nano-CMOS era—digital-assisted analog technology,” *22nd Workshop on Circuit and Systems in Karuizawa*, pp. 113–118, April 2009. (in Japanese)
- [25] H. Ito and K. Masu, “A simple through-only de-embedding method for on-wafer S-parameter measurements up to 110 GHz,” *IEEE MTT-S International Microwave Symposium 2008 (IMS 2008)*, pp. 383–386, June 2008.
- [26] S. Amakawa, H. Ito, N. Ishihara, and K. Masu, “A simple de-embedding method for characterization of on-chip four-port networks,” *Advanced Metallization Conference (AMC)*, San Diego, pp. 105–106, Oct. 2008.
- [27] S. Amakawa, K. Yamanaga, H. Ito, T. Sato, N. Ishihara, and K. Masu, “S-parameter-based modal decomposition of multiconductor transmission lines and its application to de-embedding,” *International Conference on Microelectronic Test Structures (ICMTS)*, pp. 177–180, April 2009.
- [28] S. Amakawa, T. Uezono, T. Sato, K. Okada, and K. Masu, “Adaptable wire-length distribution with tunable occupation probability,” *Int. Workshop on System Level Interconnect Prediction (SLIP)*, pp. 1–8, April 2007.
- [29] H. Ito, J. Inoue, S. Gomi, H. Sugita, K. Okada, and K. Masu, “On-chip transmission line for long global interconnects,” *IEEE International Electron Devices Meeting (IEDM)*, pp. 677–680, Dec. 2004.
- [30] H. Ito, M. Kimura, K. Miyashita, T. Ishii, K. Okada, and K. Masu, “A bidirectional- and multi-drop-transmission-line interconnect for multipoint-to-multipoint on-chip communications,” *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 1020–1029, April 2008.
- [31] H. Ito, M. Kimura, K. Okada, and K. Masu, “A 8-Gbps low-latency multi-drop on-chip transmission line interconnect with 1.2-mW two-way transceivers,” *IEEE Symp. VLSI Circuits*, pp. 136–137, June 2007.
- [32] H. Ito, J. Seita, T. Ishii, H. Sugita, K. Okada, and K. Masu, “A low-latency and high-power-efficient on-chip LVDS transmission line interconnect for a RC interconnect alternative,” *IEEE International Interconnect Technology Conference (IITC)*, pp. 193–195, June 2007.
- [33] K. Okada, H. Ito, and K. Masu, “On-chip differential-transmission-line (DTL) interconnect for 22 nm technology,” *Advanced Metallization Conference (AMC)*, pp. 2–3, San Diego, CA, Oct. 2006; *Advanced Metallization Conference, Asian Session (ADMETA)*, Tokyo, pp. 124–125, Sept. 2006; *MRS Proceedings: Advanced Metallization Conference 2006*, pp. 29–33.
- [34] T. Maekawa, H. Ito, and K. Masu, “An 8 Gbps 2.5 mW on-chip pulsed-current-mode transmission line interconnect with a stacked-switch Tx,” *34th European Solid-State Circuits Conf.*, pp. 474–477, Sept. 2008.
- [35] K. Miyashita, T. Ishii, H. Ito, N. Ishihara, and K. Masu, “An over-12-Gbps on-chip transmission line interconnect with a pre-emphasis tech-

- nique in 90 nm CMOS,” *17th Conference on Electrical Performance of Electronic Packaging (EPEP)*, pp. 303–306, Oct. 2008.
- [36] G. Chen, H. Chen, M. Haurylau, N. A. Nelson, D. H. Albonesi, P. M. Fauchet, and E. G. Friedman, “On-Chip Copper-Based vs. Optical Interconnects: Delay Uncertainty, Latency, Power, and Bandwidth Density Comparative Predictions,” *IEEE International Interconnect Technology Conference (IITC)*, San Francisco, pp. 39–41, June 2006.
- [37] N. Miura, Y. Kohama, Y. Sugimori, H. Ishikuro, T. Sakurai, and T. Kuroda, “A high-speed inductive-coupling link with burst transmission,” *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 947–955, March 2009.
- [38] W. Moriyama, K. Kimoto, S. Kubota, N. Sasaki, and T. Kikkawa, “Characteristics of Si on-chip integrated antennas fabricated on dielectric substrates,” *Ext. Abs. 2008 Int. Conf. Solid State Devices and Materials (SSDM)*, pp. 72–73, Sept. 2008.
- [39] S. Shigematsu, H. Morimura, T. Shimamura, T. Hatano, N. Ikeda, Y. Okazaki, K. Machida, and M. Nakanishi, “Logic and analog test schemes for a single-chip pixel-parallel fingerprint identification LSI,” *IEICE Trans. Electron.*, vol. E90-C, no. 10, pp. 1892–1899, Oct. 2007.

1 Introduction

Metal-oxide semiconductor field-effect transistors (MOSFETs) have been miniaturized according to a scaling scheme [1]. The scaling tendency is toward higher speeds, lower power consumption, and area reduction, resulting in cost reductions. It is noted that cost reductions cannot be expected without a reduction in chip area using miniaturized devices, when producing the same functionality. Process [2] and material developments as well as physical design are big challenges in the development of nano-complementary metal-oxide-semiconductor (CMOS) large-scale integration (LSI). In recent years, our research group has been engaged in the physical design for nano-CMOS circuits. This paper describes our recent results *vis-à-vis* variation-aware design, RF CMOS, and interconnection challenges. An ingenious method for measuring the variability of subthreshold characteristics is introduced in section 2. In section 3, recent RF CMOS issues are discussed with reference to our recent results. An on-chip transmission line interconnect developed for global wiring is discussed in section 4.

2 Variation-aware design

LSI circuit operation is strongly affected by variations in device performance, which become large as the device size is miniaturized. Taking measurements and achieving understandings of such variation are first steps in developing a variation-aware circuit design. Comprehensive work has been undertaken by STARC [3], using a device matrix array; research into understanding performance variation is continuing [4], resulting, for example, in a new V_{th} variation plot called the “Takeuchi plot.” Measurements of the saturation and the linear region current using the device array have been well studied. On the other hand, device arrays that accurately measure the I-V

curve of the subthreshold region have been scarcely reported, despite the fact that subthreshold characteristics directly affect the total power dissipation of low-threshold, high-performance circuits and the circuit performance of subthreshold circuits that operate in the subthreshold region of an MOS transistor. The measurement of subthreshold current is significantly different from that of saturation or linear region currents, owing to its low signal-to-noise (S/N) ratio, or current ratio. Here, the current ratio is defined as the target device (DUT) current, divided by the sum of non-selected DUT (NDUT) current.

We have proposed and developed MOS transistor arrays suitable for characterizing subthreshold current [5]. A key feature therein is an array containing 1,023 MOSFETs; it was carefully designed to contain the following characteristics: (1) leakage current cut-off switches (LCS) were adopted to isolate non-selected DUTs from the selected DUT; (2) the potential equalizing supply (PES) was introduced to eliminate leakage via LCS; and (3) the masking current cancellation (MCC) technique was introduced, to further improve measurement accuracy. The S/N ratio is predicted to improve from 70 without LCS/PES/MCC to 10^8 with LCS/PES/MCC, where S/N ratio is defined as the ratio of the total current of the DUT array to the current through the target DUT.

A device array with the proposed circuit was fabricated using a 90-nm, seven-metal layer CMOS process. Fig. 1 shows a chip micrograph. The total area of the circuit is $2,250 \times 1,470 \mu\text{m}$. The circuit consists of two nMOS and two pMOS arrays, and each comprises a 16×16 matrix unit (MU). Four MUs share a current measurement pad set, i.e., the subthreshold characteristics of 1,024 DUTs can be measured. In Fig. 1, one DUT is left unoccupied, so that the total masking current can be evaluated. As DUT, high-performance, low-threshold voltage transistors are utilized. The subthreshold current measurement of low-threshold voltage transistors using a device array structure

Process	90-nm CMOS, 7-Metal, triple-well
Area	$2250 \times 1470 \text{ mm}^2$
DUT size variations	16 sizes (pMOS), 24 sizes (nMOS), 256 DUT each. 1023 DUT share current-measurement pad set.
DUT pitch	$8.72 \times 13.78 \text{ mm}$ (nMOS)

Fig. 1. A chip of an array-based measurement circuit for subthreshold characteristics.

Fig. 2. (a) Measured subthreshold characteristics with and without LCS/PES/MCC. (b) Histogram of off-leakage current of different gate length transistors.

is extremely difficult, since the current of a DUT is easily overwhelmed by the masking current. Without the use of the proposed array structure, off-state current measurement is impossible.

Fig. 2 (a) shows I-V curves of the conventional and proposed arrays; each bears the same number of DUTs. In the conventional method, the current of individual devices at zero gate voltage is indistinguishable, due to the severe masking current. Threshold voltages and off-state leakage currents, both of which are obtained by extrapolation, are inaccurate; on the other hand, by using the proposed method, the subthreshold I-V curves are successfully measured. Fig. 2 (b) shows off-leak current histograms of the 32 chips on a wafer, where the off-leak current is defined by the drain current at gate voltage $V_{gg} = 0$ V and drain voltage $V_{dd} = 1.0$ V. We understand that the distribution is log-normal and that measurement correctly reflects a general trend, *i.e.*, the shorter the gate length is, the larger the current spread becomes.

More accurate and comprehensive studies *vis-à-vis* the measurement and evaluation of the performance variation of MOS transistors should be undertaken. Data thereof would be used in statistical performance modeling and novel timing analysis, including statistical static timing analysis

(SSTA) [6, 7]. The application of statistical analysis and modeling to design—and especially variation-aware design—is essential to the ultimate integration of miniaturized nano-CMOS circuits.

3 RF CMOS circuit design

3.1 RF CMOS

The RF CMOS application originates from high-frequency performance improvements in miniaturized MOS transistors as shown in Fig. 3. The cut-off frequency (f_t) at which the current gain reaches unity, as well as the maximum frequency of oscillation (f_{max}) at which the unilateral power gain reaches unity, has each grown to be > 100 GHz. When these frequencies became over several tens of GHz, the RF CMOS began to be used in GHz applications, such as in cellular phones in the 1990s. Progress on the internet requires continuously higher-speed data transfers, as well as easily made connections between users and the network; wireless access is, of course, the most convenient. There are various kind of wireless communication standards that are currently in use, including mobile phone (2G, 3G, 3.xG, etc.), WLAN (WiFi), WMAX, Bluetooth, GPS, DTV, and RFID. Multi-mode mobile phones have become popular; the three-band cellular phone is presently available, and a six-band cellular phone will be realistic within several years. Multi-mode and multi-band formats have become essential.

Fig. 3. Cut-off frequencies of various devices, and the frequency required for personal communication. The values attached to MOS data points include MOSFET technology nodes, which is almost the same as the first metal pitch. MOSFET supply voltage is also plotted.

The demands for high performance, low power consumption, and low cost are seemingly boundless with regards to communication LSI. Although super-heterodyne architecture has been utilized in RF front-end circuits for some time, it requires the use of an IF filter, which cannot be implemented on a chip. Recently, direct conversion architecture [8] has come to be widely used with a view to one-chip implementation. Although the miniaturization of MOSFET has opened the door to RF CMOS applications in the GHz fre-

quency range, there are various issues surrounding RF/analog circuit design, including the insufficient performance of on-chip inductors, the large area of on-chip passives, and design difficulties with regards to low supply voltage operation.

Thus far, in our research group, reconfigurable RF CMOS circuits for multi-band/multi-mode applications have been proposed [9, 10]; wide-band VCO and LNA as well as high-performance passives have been reported [11, 12, 13, 14]. In this section, we introduce our recent work pertaining to high-performance VCO using a high-Q WLP (Wafer-Level Packaging) inductor. Furthermore, the issues and challenges surrounding RF CMOS circuits are discussed.

3.2 High-performance VCO with high-Q WLP inductor

Conventional LC-VCO performance parameters—such as phase noise and power consumption—are directly affected by the Q-values of the LC tank. In general, Q-value of the varactor is around 50, which is much higher than that of the on-chip inductor. The inductance of the inductor for GHz-range-operated VCO is around several nH. The Q-values of an on-chip inductor is 3–5 without the RF option, and 10–15 with the RF option, where a thick $\sim 3\text{-}\mu\text{m}$ metal layer is used in the RF option. The key origins of poor Q-value are the metal resistance of the inductor itself and the resistive loss of Si substrate. If the substrate has zero or infinity resistivity, there is no resistive loss. The resistivity of the Si substrate for a standard CMOS process is several Ωcm , resulting in an eddy current loss of the substrate.

Recently, several approaches have been reported, each of which improves the Q-values of inductor and RF circuit performance using a post-CMOS process [15, 16]. We have proposed the use of WLP inductors to improve RF CMOS performance [17, 18, 19]. The WLP process is categorized in the packaging process; in the WLP process, the pad of the CMOS chip and the solder bump are connected by multilayered thick Cu metal, as shown in Fig. 4 (a). Additionally, the WLP inductor has two key features: (1) the thickness of the inductor metal is several μm , which reduces metal resistance, and (2) the distance between the inductor and the Si substrate is $> 20\text{ }\mu\text{m}$, which reduces the eddy current loss of the Si substrate. The resin used in this work has a dielectric constant of 3.2 and a dielectric loss of 0.01 at 1 GHz. Fig. 4 (b) provides a comparison of the Q-values of WLP and on-chip inductors in differential mode; the inductance of those inductors are almost the same, but the Q-value of the WLP inductor is around 40, which is much higher than that of the conventional on-chip inductor. It is also noted that the WLP process involves a low-cost packaging process, so the use of a WLP process is suitable for improving RF CMOS circuit performance with the standard, mature, and low-cost CMOS process.

We have fabricated an LC-VCO using a WLP inductor as shown in Fig. 5 [18, 19]. As a reference, an LC-VCO using a conventional on-chip inductor was also fabricated. The process technology was a $0.18\text{-}\mu\text{m}$ CMOS with an RF option. The inductors used have the characteristics shown in

Fig. 4. (a) Cross-section of WLP (Wafer-Level Packaging), and (b) Q-values of the WLP and conventional on-chip inductors. The on-chip inductor is fabricated by a 0.18-μm CMOS with a thick-metal option. The inductance values of the WLP and conventional inductors are 3.5 nH and 4.2 nH, respectively.

Fig. 5. LC-VCO with high-Q WLP inductor. (a) Circuit. (b) VCO core without WLP inductor. (c) VCO with WLP inductor. A 180 nm CMOS process was used.

Fig. 3. Fig. 6 shows the phase noise characteristics and provides a performance summary. The phase noise of the VCO with a WLP inductor was -134.4 dBc/Hz at a 1-MHz offset for a 1.91-GHz carrier frequency. The conventional VCO (reference) had a phase noise of -128.0 dBc/Hz for a 1.92-GHz carrier frequency. The VCO with a WLP inductor improves the phase noise

	The proposed VCO	On-chip VCO
Supply voltage	1.8V	1.8V
Oscillation Freq.	1.91GHz	1.92GHz
Process	180nm CMOS+WLP	180nmCMOS
Power dissipation	5.7mW	5.7mW
Phase noise @1MHz offset	-134dBc/Hz @1.91GHz	-128dBc/Hz @1.92GHz

$$FoM = L \{ f_{offset} \} - 20 \log \left(\frac{f_{offset}}{f_{offset}} \right) + 10 \log \left(\frac{P_{DC}}{1mW} \right)$$

Fig. 6. Phase noise characteristics and performance summary of LC-VCO with high-Q WLP and conventional on-chip inductors.

of 6.4 dB, compared to that of the reference. The figure of merit (FoM) is -193 dBc/Hz. An LNA with a high-Q WLP inductor has been also designed; in fact, an LNA with a WLP inductor has superior characteristics to that with on-chip inductors.

3.3 Issues and approaches of RF CMOS in the next generation

In this section, issues related to current RF CMOS circuits as well as approaches to next-generation RF CMOS circuit integration are discussed.

The miniaturization of MOSFET according to scaling has brought about great changes in digital domain circuits and systems. Miniaturization is synonymous with high speed, low power consumption, and low cost, all of which are driven by reductions in chip area. Process technology progress has also greatly impacted analog circuit performance improvements. In analog and RF circuits, passive components such as resistors, capacitors, and inductors are implemented. The introduction of a metal-insulator-metal (MIM) capacitor using high-k material is benefitted from the improvement of the process technology. However, the scaling situations differ from those of digital circuits.

The use of direct-conversion architecture has become popular in the creation of RF CMOS circuits, and a one-chip RF front-end is available. One therefore expects the possibility of a one-chip solution, where RF front-end, digital baseband modulation and demodulation, and base band digital processing are integrated into one chip. However, the values of the passive com-

ponents of an RF front-end circuit remain unchanged when the operation frequency range is not changed; this means that the area of passives are not scaled, *i.e.*, the total chip area—including RF, analog, and digital circuits—cannot be sufficiently reduced. There are scalability difficulties, including the cost of scaling in RF, analog, and digital SoC [20]. Furthermore, since there are other approaches—such as SiP, 3D-SiP and 3D integration—an on-chip solution (SoC) is not always the best solution.

Passives such as capacitor and inductor are still important. If conventional architecture is used, a 0.18- μm /0.13- μm /90-nm mature CMOS process is sufficient in realizing GHz performance and low cost. The Q-values of passives directly affect analog/RF circuit performance; especially, improvements in the Q-value of the inductor are strongly required. Passives with variable characteristics, such as variable capacitors and variable inductors, are promising; these variable passives are useful for wide-band RF CMOS circuits and systems [10, 11]. A reduction in inductor area is a challenge; for example, as shown in Fig. 7(a), if the line impedance surrounding LNA or PA is changed, the inductance of on-chip matching inductors varies, *i.e.*, there is the possibility to reduce the inductor area.

Novel passives are promising and include MEMS switches, MEMS passives, and the like. Low-cost, reliable MEMS switches are useful for multi-band transceivers. As a novel passive, the MEMS resonator is promising, because a filter bank can be implemented in a small area of several hundred square μm [21]. Another approach using left-hand material may also be promising, if the passives' total area can be reduced.

Digital-rich and/or digital enhancement is a big challenge for miniaturizing RF CMOS circuits [22, 23, 24]. As shown in Fig. 3, supply voltage decreased with scaling; the supply voltage became < 1 volt. A decrease in supply voltage makes an analog design difficult, because neither a sufficient voltage swing nor a large range of linearity can be guaranteed. Also, device performance variation directly affects analog/RF circuit performance. There are several challenges inherent in digital signal processing, based on amplitude domain and time domain [24]. Using digital processing in an RF CMOS circuit, the use of inductors will be reduced or eliminated, resulting in area consumption decrease; however, the use of other passives such as capacitors and resistors must also be reduced.

The use of novel integration technologies with 3D integration is also a challenge. 3D stacking using conventional wire bonding is widely used in memory-stacking, and 3D stacking using TSV (Through Si Via) has become popular. 3D stacking of RF, analog, and digital chips is one way of creating small-size transceiver chips, and it uses chips designed and fabricated using mature CMOS process technology. The challenge is not only to develop 3D stacking process technology, but also to develop an EDA environment.

Making developments in tandem with JISSO technology is inherently important. RF CMOS circuits are especially important to implementation in wireless systems, such as mobile phones, WLAN cards, *etc.* System performance and cost are, of course, most important. In RF transceivers, the com-

ponents of CMOS LSIs, passives, antennae, and the like are implemented on PCB. The best implementation of an RF CMOS circuit should be discussed with an eye to system requirements. In this sense, the design environment and/or design platform—including CMOS and JISSO, *i.e.*, design environment and/or design platform of integration of diverse functionalities—becomes increasingly important.

Finally, the importance of measurement is pointed out. In RF CMOS circuit design, accurate devices and passive modeling are absolutely essential. To bring about accurate modeling, the precise measurement of GHz range is required. In the measurement of active and passive devices, the de-embedding technique becomes more important [25, 26, 27]. Modeling and measurement are also important in the design of transmission interconnects, as described in the next section.

Fig. 7 summarizes the challenges inherent in RF CMOS circuits, and some of the approaches to RF CMOS design.

Fig. 7. (a) Issues of direct conversion of RF CMOS front-end, and (b) novel technologies surrounding the RF CMOS.

4 Interconnect integration

Although device sizes have been miniaturized, chip sizes have not been reduced; interconnect delays of long wires limit digital circuit performance.

Interconnect design is a perennial issue with CMOS LSI. Our emphasis in interconnect design has been to understand the evaluation of interconnect resources and design low-latency global wiring.

There have been reports estimating the number of wires in digital circuits. Estimating the required wiring resources is essential to estimating the performance of not only conventional SoC integration, but also novel 3D integration. It has been known that interconnect length distributions all have a similar characteristic, which is characterized by the Lent parameters of k and p . Here, the interconnect length distribution is the number of interconnects, as a function of interconnect length. Previous models cannot represent both the interconnect length distribution and the cumulative number of interconnect as a function of length. Our approach is to introduce a new parameter relating to cell efficiency. The wire length distribution and the cumulative number of interconnects in commercially available chips can be successfully represented using analytic expressions [28].

For global interconnects, we have proposed the use of an on-chip transmission line interconnect (TLI), and its application to NoC (Network on a Chip). It has been demonstrated that TLI has lower latency and smaller delay-time variations than conventional RC interconnects [29, 30, 31, 32, 33]. To further improve TLI, we have recently developed the pulse current mode (PCM) circuit [34] and the equalizing technique [35]. This paper discusses the pulsed current mode circuit, which features low power consumption [34].

In an on-chip transmission line interconnect, current-mode differential-amplifiers are used for a transmitter (Tx) and a receiver (Rx) in TLIs. The power consumption of TLIs is almost solely determined by the static power consumption of Tx and Rx; it does not depend on signal frequency. These circuits are not adequate for interconnects with low activity factors or for transmitting lower bit-rate signals.

Fig. 8 shows a schematic of the proposed PCM-TLI. PCM-TLI consists of pre-buffers for generating differential signals, stacked-switch Txs, an on-chip differential transmission line (DTL), and an Rx. Rail-to-rail signals are input

Fig. 8. Pulse current mode transmission line interconnect (PCM-TLI).

Fig. 9. Simulated time-domain waveforms at 10 Gbps.

Maximum bit rate	8Gbps
Power Consumption($V_{DD} = 1.0V$, 8Gbps)	Tx:1.2 mW Rx :1.3 mW (Total : 2.5 mW)
Energy per bit	0.31 pJ/bit
Delay(w/o buffer)	164 ps
Area	Tx: $48 \times 8 \mu m^2$, Rx: $22 \times 32 \mu m^2$

Fig. 10. Point to point PCM-TLI.

into the PCM-TLI, and Txs convert rail-to-rail signals to pulse-shaped differential RZ-signals. RZ signals propagate in the DTL at an electromagnetic-wave speed. The Rx amplifies pulse signals and converts RZ signals to non-return-to-zero (NRZ) signals. A buffer is used for measurements. Using the delay circuit, Tx produces narrow pulse signals. In our work, the delay time τ is designed to be 100 ps, *i.e.*, 100 ps-pulse-width signaling. The Rx consists of a differential amplifier and a p-Schmitt trigger circuit. The differential transmission line interconnect in this work has a line-width and space of $6.0 \mu m$, and the designed differential impedance is 100Ω . Details of the operation of Tx and Rx are described elsewhere [34].

Fig. 9 shows a simulated time domain wave form of Tx. The narrow pulse is output from Tx, and the static current does not flow.

A 5-mm-long point-to-point PCM-TLI is fabricated by using a 90-nm CMOS process. Fig. 10 shows a chip micrograph, a measured eye pattern of output signal from the buffer at 8 Gbps, and a performance summary. The maximum bit rate was 8 Gbps when the eye-width margin was assumed to be $> 20\%$ of the period at a bit-error rate of 10^{-12} . In this circuit, the maximum bit rate is found to be limited by the buffer.

Fig. 11 (a) shows power consumption as a function of bit rate. The consumption of conventional TLIs does not depend on bit rate; on the other hand, the power consumption of PCM-TLIs is proportional to bit rate, *i.e.*,

Fig. 11. Pulse current mode transmission line interconnect (PCM-TLI). (a) power consumption as a function of bit rate, and (b) delay vs. energy per bit of various circuits.

power consumption is reduced at a low bit rate. Fig. 11 (b) summarizes the delays of various interconnects as a function of energy per bit. As shown in this figure, the TLIs that have been developed in our group have low delays with low bit energy.

We have proposed an FoM for on-chip interconnects [33]. The FoM is defined as

$$FoM = L^3/E \cdot D^2 \quad \dots \quad (1)$$

where L [mm] is line length, E [pJ] is the energy loss in signal transmission, and D [ps] is the delay. A small delay and low energy-dissipation interconnect therefore obtains a high FoM. Energy loss E is proportional to the product of P and D ; for the RC line, P and D are also proportional to line length L . The ED products of the RC lines are proportional to the cube of L , so that the FoM of the RC lines becomes constant.

Fig. 11 summarizes the FoMs of several interconnection techniques, as functions of line length: DTL interconnects in 90 nm and 22 nm, RC interconnects in 90 nm and 22 nm, and CNT (Carbon Nano Tube) interconnects in 22 nm. There are also optical interconnects. In the CNT interconnect, the line consists of an ideal CNT. The optical interconnect is assumed to consist of an optical modulator, a modulator driver, a waveguide, a photo detector, an amplifier, and an external laser as a light source [36]. The detailed as-

sumptions are described in Okada *et al.* [33]. One of the biggest differences between electrical and optical interconnects is in signal loss. Optical interconnects do not require repeaters. The FoM of RC interconnects is saturated because of an enormous number of repeaters; the FoM of DTL is also saturated around 100 mm, which depends on signal attenuation as determined by the wire structure.

As expected, the RC line has a superior FoM in terms of its short length (*i.e.*, below hundreds of μm (local wiring)); the optical interconnect has a superior FoM in terms of its long interconnect length (*i.e.*, more than several cm). This means that the DTL interconnect is preferred for global interconnects that are mm or cm long.

Furthermore, novel interconnect technologies—such as 3D stacking that uses conventional wiring or TSV—and proximity wireless interconnects [37, 38] have been developed. These interconnect technologies are suitable for the integration of diverse functionalities. To compare the performance of these electrical and optical interconnect techniques, more detailed discussion is required. For example, one should propose a novel FoM that considers the interconnect area and driver/receiver circuit. This FoM would be helpful in discussing the usefulness of 3D integration.

Fig. 12. FoM (Figure of Merit) of various interconnects. RC: conventional RC; CNT: interconnect using carbon nano-tube; DTL: differential transmission line; OPT: optical interconnect. Numerals represent the CMOS technology generation of the circuit. For example, “RC90” refers to an RC interconnect that uses a 90-nm CMOS process.

5 Conclusion

In this paper, we described our recent work with regards to the physical design of CMOS circuits. At the present time, one can use multi-generation CMOS processes. There are many challenges in producing nano-CMOS circuits, such as how to design circuits with device characteristic variability, how to design RF CMOS using highly miniaturized CMOS with a very low supply voltage of $< 1\text{ V}$, *etc.* On the other hand, although a sub-100-nm CMOS

is now widely available, $1.2\mu\text{m}/0.8\mu\text{m}$ CMOS processes as well as mature submicron CMOS processes are still available. Furthermore, 3D stacking or ultra-fine JISSO technology has become popular. This means we have many choices when implementing systems. It will become more important to understand which integration scheme is best for a given need, or how to determine the best choice, *e.g.*, SoC solution using advanced CMOS, or 3D or SiP integration using the mature CMOS. Finally, the authors would like to emphasize again that the design environment or integrated design platform become more important for the integration of diverse functionalities.

Acknowledgments

The research in this paper was partially supported by JSPS.KAKENHI, MEXT.KAKENHI, STARC, NEDO, SCOPE, and MIRAI/NEDO. The authors thank the corporations that financially support our research: Fujikura, NEC, Mitsubishi Electric, Fujitsu, Oki Electric, Murata, and Intel. Regarding chip design and fabrication in this work, we are indebted to VDEC, in collaboration with Cadence Design Systems, Inc. and Synopsys, Inc. The authors thank Associate Professor Kenichi Okada and Assistant Professor Hiroyuki Ito for their great contribution to our research activities. The authors are also indebted to the graduate school students of our research group for their contributions, especially in providing chip design assistance and evaluations while concurrently preparing Masters and Doctoral thesis work.

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