FeCMOS logic inverter circuits with nonvolatile-memory function

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Abstract: Operations of ferroelectric complementary metal-oxide-semiconductor (FeCMOS) circuits, which are composed of ferroelectric-gate field effect transistors (FeFETs) instead of conventional MOS FETs, are demonstrated for the first time. The FeCMOS circuits have a practical value of saving much power consumption by switching the circuit function between logic and distributed nonvolatile memory. The function switching is possible by momentary expanding supplied voltages before cutting the power-supply. We fabricate FeCMOS inverters as representative logic elements and demonstrate the function switching from logic to nonvolatile memory. As the nonvolatile memory, accurate operations of data write, sleep with no supplied voltages and nondestructive read, are verified. The nonvolatility is confirmed by output-voltage retention measurements.

Keywords: FeCMOS, FeFET, nonvolatile logic

Classification: Integrated circuits

References


1 Introduction

Logic circuits with nonvolatile-memory function, which are called nonvolatile logic circuits, have attracted much interest for application to next-generation mobile devices with high-speed and low-power consumption. Several types of the nonvolatile logic using ferroelectric capacitors [1] and magnetic tunnel junctions [2] have been reported. As another type of the nonvolatile logic, we propose ferroelectric complementary metal-oxide-semiconductor (FeCMOS) circuits which are CMOS circuits composed of ferroelectric-gate field effect transistors (FeFETs) instead of conventional MOS FETs. The FeFETs are well-known as memory transistors which include ferroelectric materials in the gate insulators. The FeFETs have both n-channel-type (n-ch) and p-channel-type (p-ch) as conventional MOS FETs have. Since a good data retention of an FeFET has been demonstrated [3], device reliabilities [3, 4, 5] and threshold voltage controls [6, 7] of FeFETs have been intensively studied. Previously, we have introduced basic logic and memory operations of a single-stage inverter composed of FeFETs by directly changing of the gate-input signal amplitude [8]. In this study, we demonstrate an advanced usage of the FeCMOS. That is function switching from logic to nonvolatile memory by changing supplied voltages. The FeCMOS needs to be supplied with dual high and low voltages for adding nonvolatile memory function to the conventional logic operation. No area penalty for preparing ferroelectric capacitors and no power loss by using resistors as compared with the other proposed nonvolatile logic circuits. The FeCMOS may enable us to realize quick-on-and-off computers or digital electronic devices with ultra-low power consumptions.

2 Principles of FeCMOS operation

An FeFET works as a logic transistor or a conventional MOS transistor when a voltage difference between the gate and the substrate ($V_{\text{g-sub}}$) is small enough to show negligibly narrow memory windows in drain current ($I_d$)-$V_{\text{g-sub}}$ curves. On the other hand, the FeFET works as a nonvolatile
memory transistor when the $V_{g-sub}$ is large enough to show wide memory windows in the $I_d-V_{g-sub}$ curves. In order to explain the FeCMOS function switching from the logic to the memory only by changing the supplied voltages, we use a double-stage FeCMOS inverter as shown in Fig. 1(a). High and low voltages supplied to the first stage are $V_{H1}$ and $V_{L1}$. Those supplied to the second stage are $V_{H2}$ and $V_{L2}$, respectively. A series of operations of the double-stage inverter in Fig. 1(a) such as logic, data write, sleep with no power supplied, nondestructive read and logic again, are as follows and shown in Fig. 1(b).

In logic operation, digital input signal $V_{in}$ is swung between $V_{cc0}$ and $V_{ss0}$ under high and low supplied voltages of $V_{H1} = V_{H2} = V_{cc0}$ and $V_{L1} = V_{L2} = V_{ss0}$. In this case, $V_{g-sub}$s of the two p-ch FeFETs are either $0$ V or $V_{ss0}$-$V_{cc0}$. Those of the other two n-ch FeFETs are either $V_{cc0}$-$V_{ss0}$ or $0$ V. The n- and p-ch FeFETs show the $I_d-V_{g-sub}$ curves with very narrow memory windows at the $V_{g-sub}$ ranges from $|V_{ss0}$-$V_{cc0}|$ to $0$ V.

![Double-stage FeCMOS inverter diagram](image)

**Fig. 1.** (a) Double-stage FeCMOS inverter and (b) how to operate the circuit.

In write operation, $V_{H1}$ is increased from $V_{cc0}$ to $V_{cc1}$ and $V_{L1}$ is decreased from $V_{ss0}$ to $V_{ss1}$, while $V_{H2} = V_{cc0}$ and $V_{L2} = V_{ss0}$. When the input is high or $V_{in} = V_{cc0}$, the p- and n-ch FeFETs in the second-stage inverter have expanded $V_{g-sub}$s of $V_{g-sub} = V_{ss1}$-$V_{cc0}$ and $V_{g-sub} = V_{ss0}$-$V_{ss1}$, respectively, if the threshold voltages ($V_{th}$s) are well adjusted. In this case, the p-ch FeFET
will memorize on-state and the n-ch FeFET will memorize off-state in the second-stage inverter. When the input is low or $V_{in} = V_{ss0}$, the p- and n-ch FeFETs in the second-stage inverter have oppositely expanded $V_{g-sub}$. In this case, the p-ch FeFET will memorize off-state and the n-ch FeFET will memorize on-state in the second-stage inverter. While $V_{H1} = V_{cc1}$ and $V_{L1} = V_{ss1}$, $V_{in}$ should become 0 V before all the supplied voltages go down to 0 V in order to avoid a memory error.

In sleep operation, no signal is input, $V_{in} = 0$ V, and no voltages are supplied, $V_{H1} = V_{H2} = V_{L1} = V_{L2} = 0$ V.

In nondestructive read operation, only $V_{H2} = V_{cc0}$ and $V_{L2} = V_{ss0}$, while $V_{H1} = V_{L1} = 0$ V. No signal is input, $V_{in} = 0$ V. Whether high or low $V_{out}$ will be read out depends on what states have been memorized in the FeFETs in the second-stage inverter. For example, if the memorized states of the p- and n-ch FeFETs in the second-stage inverter are on and off respectively, $V_{out} = V_{cc0}$ is obtained. This read operation is nondestructively repeatable.

In logic operation again, all the supplied voltages are restored, $V_{H1} = V_{H2} = V_{cc0}$ and $V_{L1} = V_{L2} = V_{ss0}$, and $V_{in}$ resumes receiving signals.

### 3 Experimental results

We fabricated and measured the double-stage FeCMOS inverter drawn in Fig. 1 (a) using Pt/SrBi$_2$Ta$_3$O$_9$(SBT)/(HfO$_2$)$_{0.75}$(Al$_2$O$_3$)$_{0.25}$(HAO)/Si. The fabrication process was described before [4]. Dual voltages were prepared for high and low, individually. $V_{cc0}$ and $V_{ss0}$ were $-0.3 \pm 1.0$ V, or $V_{cc0} = 0.7$ V and $V_{ss0} = -1.3$ V. $V_{cc1}$ and $V_{ss1}$ were $-0.3 \pm 3.4$ V, or $V_{cc1} = 3.1$ V and $V_{ss1} = -3.7$ V. The FeFETs we fabricated in this study had the center voltage of $-0.3$ V, which was controllable by changing channel ion-doping condition. By adjusting the condition properly, the center voltage would be 0 V.

The operations explained in the previous chapter were all cleared. Figure 2 (a) shows the $V_{out}$ retention characteristics, which were obtained by
plotting $V_{\text{out}}$ by the nondestructive read operations. The retention times, which were times integrated from the end of the data write, were measured up to 30.5 hours for the high $V_{\text{out}}$ and 41 hours for the low $V_{\text{out}}$. Figure 2 (a) indicated that the high $V_{\text{out}}$ of almost 0.7 V, or $V_{\text{cc}}$, and the low $V_{\text{out}}$ of almost $-1.3$ V, or $V_{\text{ss}}$, were successfully read out throughout such long times. We prepared a probe pad connected to the intermediate node of the double-stage FeCMOS inverter. A $V_{\text{out}}$-memory window was investigated by sweeping the intermediate-node voltage $V_{n0}$ (Fig. 1 (a)) between sufficiently small voltages $-0.3$ V and 0.3 V. The memory window just after high- and low-data write operations was about 0.2 V which was obtained by measuring $V_{\text{out}}$-$V_{n0}$ curves as shown in Fig. 2 (b). The left and right $V_{\text{out}}$-$V_{n0}$ curves of the memory window should be positioned symmetrically with respect to the line of $V_{n0}$ = 0 V for retaining reliable $V_{\text{out}}$ memories with no supplied voltages and for making high- and low-$V_{\text{out}}$ retention times almost equal.

4 Discussions

As we demonstrated above, FeCMOS function was switched from logic to nonvolatile memory by changing supplied voltages. The double-stage inverter was introduced as an example of very familiar logic. In a practical use, the FeCMOS will be probably used mostly as a conventional logic and occasionally as nonvolatile memory. We investigated pulse endurance of $V_{\text{th}}$ of n-ch Pt/ SBT/HAO/Si FeFETs with $L = 10 \mu$m as shown in Fig. 3 (a). An FeFET was used for the endurance correspond to on- and off-state memory operations. They were measured by applying $1.1 \times 10^{11}$ cycle pulses of $1 \pm 4$ V at 4 MHz. The amplitude 4 V was large for the FeFET enough to show a wide memory window of about 0.8 V. The pulse endurance correspond to logic operation was also measured using another FeFET by applying $1.6 \times 10^{12}$ cycle pulses of $2 \pm 0.6$ V at 10 MHz. The amplitude 0.6 V was small.

![Fig. 3](image)

**Fig. 3.** (a) $I_{d}$-$V_{g\text{-sub}}$ curves measured for obtaining pulse endurance of $V_{\text{th}}$. (b) Pulse endurance characteristics of two memorized states of an FeFET with large applied voltage-range $1 \pm 4$ V and one non-memorized state or logic-transistor state of an FeFET with small applied voltage-range $2 \pm 0.6$ V.
for the FeFET enough to show a negligibly narrow memory window. When
the $V_{g\text{-sub}}$ sweeping range was $1 \pm 4$ V, the $V_{\text{th}}$ shifted 5% after on-memorized
by $V_{g\text{-sub}} = 5$ V and 2% after off-memorized by $V_{g\text{-sub}} = -3$ V at the pulse
repetition number of $1.1 \times 10^{11}$ as shown in Fig. 3 (b). When the $V_{g\text{-sub}}$ range
was $2 \pm 0.6$ V, the $V_{\text{th}}$ shifted only 1% even at the pulse repetition number of
$1.6 \times 10^{12}$. The results indicated that FeCMOS meets the needs of prospective
nonvolatile logic circuits for saving power consumption, which will be used
mostly as a conventional logic with small applied voltages and occasionally
as a nonvolatile memory with large applied voltages.

5 Conclusion

As novel type of the nonvolatile logic, we propose FeCMOS circuits which are
CMOS circuits composed of FeFETs instead of conventional MOS FETs. The
unique characters of the FeFETs were used, which are working as logic tran-
sistors by small applied voltages and as nonvolatile memory transistors by
sufficiently large applied voltages. As an example of the FeCMOS, a double-
stage inverter circuit was fabricated for demonstrating a series of regular
operations such as data write, sleep with no supplied voltages and nonde-
structive read. The FeCMOS function switching from the logic to the mem-
ory was successfully demonstrated only by changing the supplied voltages
just before the following sleep operation. The retention times of the FeC-
MOS circuits were measured up to 30.5 hours for the high $V_{\text{out}}$ and 41 hours
for the low $V_{\text{out}}$. Pulse endurances of n-ch FeFETs correspond to two memo-
rized states were measured by applying $1.1 \times 10^{11}$ cycle pulses of $1 \pm 4$ V. At
the applied pulse number $1.1 \times 10^{11}$, the $V_{\text{th}}$ shifted 5% after on-memorized
and 2% after off-memorized. Endurance correspond to logic operations were
also measured by applying $1.6 \times 10^{12}$ cycle pulses of $2 \pm 0.6$ V. Very small
$V_{\text{th}}$ shift of only 1% was obtained even after such a large number of pulses
applied. The results indicated that FeCMOS meets the needs of prospective
nonvolatile logic circuits for saving power consumption, which will be used
mostly as a conventional logic and occasionally as a nonvolatile memory on
demand.

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