New low-voltage small-area mixed-voltage I/O buffer

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Abstract: A new mixed-voltage I/O buffer having the characteristics of low-voltage operation and small-area realization is proposed. The proposed I/O buffer provides significantly reduced latency at low supply voltages by eliminating the voltage swing degradation at timing-critical nets. The buffer also provides smaller layout area by avoiding the use of dedicated extra circuits like dynamic gate-bias circuit (DGBC) and hot-carrier prevention circuits (HCPC) to cope with hot-carrier-induced gate-oxide reliability issue. Comparison results in an 80-nm CMOS process indicate that the proposed mixed-voltage I/O buffer achieves 73% reduction on buffer latency, 23% reduction on operating voltage, and 31% reduction on layout area as compared to conventional I/O buffers.

Keywords: I/O buffer, mixed-voltage, hot-carrier injection, low voltage, area reduction

Classification: Integrated circuits

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1 Introduction

In a microelectronic system composed of ICs powered by different supply voltages, the use of conventional non-mixed-voltage I/O buffers can cause serious problems such as undesirable short-circuit current, junction-leakage current, and hot carrier-induced gate-oxide reliability issue [1]. For example, a substantial amount of short-circuit current can flow from an I/O pad of such an IC to the power supply in the case that the voltage level of the I/O pad driven externally is higher than the supply voltage of the IC. The junction-leakage current can also occur at the drain-well junction of the pull-up pMOS transistor in the buffer when a signal voltage driven externally to the I/O pad is higher than the well bias. The gate-oxide reliability issue induced by hot-carrier injection can occur when any transistor in the buffer is turned on with too large voltage difference between the drain and source and between the gate and source.

For addressing the issues aforementioned, several I/O buffers using mixed voltages have been proposed [1, 2, 3]. To eliminate undesirable short-circuit and junction-leakage currents, a mixed-voltage I/O buffer adopting a gate-tracking method and a dynamic n-well bias scheme has been proposed [1]. However, this scheme requires many extra transistors having complicated connections. To avoid the gate-oxide reliability problem, nMOS blocking technique [2] and nMOS stacking method have been proposed. But, operated in ultra-low voltage region, the use of these transistors can limit the voltage swing of received input, severely degrading the receiving speed. Moreover, they still suffer from the hot-carrier injection problem during transition intervals from a receiving mode to a transmit mode. For avoiding the hot-carrier injection during transition intervals, a mixed-voltage I/O buffer having hot-carrier prevention circuits has been proposed [3]. However, the circuit still has a large area penalty and a limited operating voltage.

In this paper, a new mixed-voltage I/O buffer is proposed to avoid several issues described previously and to support a reliable operation at lower supply voltage. Analysis for conventional mixed-voltage techniques is reviewed in section II. The proposed mixed-voltage I/O buffer is described in section III. Section IV presents comparison results, and conclusions are given in section V.

2 Conventional mixed-voltage I/O buffers

The conventional mixed-voltage I/O buffer using nMOS blocking technique [2] is shown in Fig. 1 (a). The gate voltage of nMOS blocking transistor MN0 located between DIO and the I/O pad is controlled by a dynamic gate-bias circuit (DGBC). DGBC prevents signal-level degradation and gate-oxide reliability problem by forcing the gate voltage of MN0 to V_{DDH} ($2V_{DD}$) for an outgoing high data and to V_{DD} for an outgoing low data during the transmit mode. DGBC also avoids short-circuit and junction-leakage currents through MP0 for receiving a high data ($2V_{DD}$) by making the gate of MN0 biased at V_{DD} during the receiving mode. However, one major drawback of using

Fig. 1. (a) Conventional mixed-voltage I/O buffer using nMOS blocking technique [2], and (b) conventional mixed-voltage I/O buffer with hot-carrier prevention circuits [3].

DGBC is that the latency of it causes the buffer to have an increased overall transmit delay. The use of DGBC also causes the signal-level degradation of received logic high data at DIO, resulting in significantly increased receive delay especially when the supply voltage is very low. Moreover, DGBC should be placed separately in each I/O buffer, resulting in an increased area overhead. In addition, blocking transistor MN0 still suffers from the hot-carrier injection problem [3] when the I/O buffer tries to transmit a low data (GND) after receiving a high data ($2V_{DD}$).

The conventional mixed-voltage I/O buffer adopting a TG-based gate-tracking circuit [1] and hot-carrier prevention circuits (HCPC) [3] is shown in Fig. 1 (b). For avoiding hot-carrier injection in MN0, MN2/MP2, and MN3, three HCPCs are placed at the I/O pad, PU, and G2, respectively. Then, during transition intervals from a receiving mode to a transmit mode, the charges deposited at these nodes due to the previous incoming high data are transferred to the supply rail by the associated HCPC. Although the resulting settling voltages at these nodes are actually higher than V_{DD} by V_{TH} , the peak drain-source voltages of MN0, MN2, and MN3 during the transmit mode do not exceed V_{DD} since the gates of these transistors are biased at V_{DD} and the sources of them do not abruptly go to GND. However, structural complexity and area penalty of this conventional I/O buffer are high since all of these three hot-carrier prevention circuits should be duplicated in each

Fig. 2. The proposed mixed-voltage I/O buffer.

I/O buffer. Moreover, this I/O buffer still has a voltage limitation due to small voltage swing at DIO.

3 Proposed mixed-voltage I/O buffer

The proposed mixed-voltage I/O buffer is shown in Fig. 2. The buffer consists of a pre-driver, a main driver, a receiver, and a peripheral circuit (shown in the dotted box). PB, the substrate of MP0 and MP1, is driven by a level converter shifting an inverted OE from GND to V_{DD} and from V_{DD} to V_{DDH} ($2V_{DD}$). PU, the gate of MP0, is driven by the pre-driver via MN2, while PD, the gate of MN1, is directly driven by the pre-driver. Although PU is also connected to PB via MP1, signal fighting between the pre-driver output and PB does not occur since MP1 is turned on only when PU is at logic high level. G2, the gate of MN2, is driven by another level converter shifting OE from GND to V_{DD} and from V_{DD} to V_{DDM} ($V_{DD} + V_{TH}$). The gate of the stacked nMOS transistor MN0 is connected to V_{DDM} .

Let us explain the operation of the proposed mixed-voltage I/O buffer. In the transmit mode, OE becomes high, and both PU and PD together go high or low according to the logic level at DOUT, turning either MP0 or MN1 on for driving the I/O pad. During this mode, the voltage of PB stays at V_{DD} for avoiding the body effect of MP0. In the receiving mode, PU and PD stay at V_{DDH} and GND, respectively, turning MP0 and MN1 off, and then, data from the I/O pad is received by the input receiver. Note that the logic high of DIO reaches up to full V_{DD} for an incoming high data since the gate of MN0 is biased at V_{DDM} . The voltage of PB stays at V_{DDH} during this mode for preventing the undesirable drain-well junction-leakage current through MP0. The voltage of G2 stays at V_{DD} for preventing the undesirable short-circuit current through MN2. During transition periods from a receiving mode to a transmit mode, in which OE is enabled and the pre-driver is not yet activated, residue charges deposited at PU and the I/O pad due to previous incoming high data are eliminated and the voltages of them settle at V_{DD} and $V_{DD} + V_{TH}$, respectively. Although the settling voltage of I/O pad is somewhat higher than V_{DD} , the drain-source voltage of MN0 during the transmit mode never exceeds V_{DD} since the gate of this transistor is biased at

V_{DDM} and the source of this transistor does not abruptly go GND, resulting in no hot-carrier injection.

The proposed mixed-voltage I/O buffer has several important advantages as compared to conventional mixed-voltage I/O buffers. As seen previously, the logic high of the received signal at DIO always reaches at V_{DD} , allowing the voltage swing to be larger by V_{TH} than those of the conventional buffers. (Note that, for the conventional buffers shown in Fig. 1 (a) and 1 (b), the logic high levels of received signal at DIO are identically $V_{DD} - V_{TH}$ since the gate of MN0 in each buffer is connected to V_{DD} .) The full-swing of received signal at DIO of the proposed buffer relieves the receiver-latency increase at low supply voltages, allowing for faster operation at low voltage region. As far as layout area is concerned, the proposed I/O buffer occupies the smallest silicon area among I/O buffers compared. The reason comes from the fact that the proposed I/O buffer uses no bulky extra circuits like DGBC and HCPC for eliminating the short-circuit and junction-leakage currents and the hot-carrier injection problem. Although the proposed I/O buffer employs instead the peripheral circuit having two level converters, the area overhead is not high because this circuit can be shared with other I/O buffers. Although the proposed buffer can have the gate-drain voltage of MP0 above V_{DD} when receiving a low data, the transistor does not enter the accelerated gate-oxide breakdown condition [4] because MP0 whose drain-source voltage is V_{DD} stays off. (For an off-state pMOS, the voltage at which gate-oxide stress occurs is known to be over twice the nominal operating voltage [5].) So, MP0 does not suffer from the gate-oxide reliability problem.

Fig. 3. Comparison results: (a) data capture time versus supply voltage, (b) received data waveforms, (c) layout area, and (d) peak drain-source voltage versus supply voltage.

4 Comparison and discussion

To verify the effectiveness of the proposed circuit, the four-bit mixed-voltage I/O buffers using the conventional [2, 3] and proposed techniques have been designed and simulated in an 80-nm CMOS process. In the conventional I/O buffer in Fig. 1 (a), an HCPC with a shared level converter is added at the I/O pad for eliminating hot-carrier injection. Each buffer has an output loading of 5 pF, and the latency of HCPC is set to be 1 ns. The voltage levels for V_{DDH} and V_{DDM} are set to be at $2V_{DD}$ and $V_{DD} + 0.4\text{ V}$, respectively. For comparing the speed performance of the I/O buffers, the capture time from the I/O pad to DIN for receiving a high data for the supply voltage ranging from 1.0 to 2.0 V are depicted in Fig. 3 (a). The data capture time of the conventional buffers in Fig. 1 (a) and (b) are 902 ps and 1004 ps at 1.2-V supply voltage, respectively, and dramatically increases at lower supply voltages. Meanwhile, that of the proposed buffer is 291 ps at 1.2-V supply voltage and 546 ps at 1.0-V supply voltage, achieving up to 73% reduction on latency at 1.2-V supply voltage, and up to 23% reduction on operating voltage for providing the same latency of 550 ps. Simulated waveforms of DIO and DIN for each buffer operating at 1.2-V supply voltage are shown in Fig. 3 (b). As seen by the figure, the rising slopes of DIO in the conventional buffers are distorted since the I/O pad ceases to drive the receive nodes at above 0.8-V signal level, making DIN have an increased latency. On the other hand, the received data at DIO of the proposed buffer reaches the high level swiftly, resulting in a much faster evaluation of DIN. To compare the area of the I/O buffers, the layout area occupied by each I/O buffer excluding the area of I/O pad are summarized in Fig. 3 (c). In the figure, ‘Driver/Receiver’ denotes the area occupied by the driver and receiver in each buffer dedicated to each I/O bit. ‘Shared peripheral’ means the area occupied by the peripheral circuit shared among four I/O bits, which are evaluated by considering one-fourth of the actual layout size. As seen in Fig. 3 (c), the total area of the proposed buffer is $1430.5\text{ }\mu\text{m}^2$, while those of the conventional I/O buffers in Fig. 1 (a) and 1 (b) are $2064.5\text{ }\mu\text{m}^2$ and $1803.5\text{ }\mu\text{m}^2$, respectively, indicating up to 31% reduction. This area reduction mainly comes from no use of bulky extra circuits like HCPC and DGBC. To compare the immunity to hot-carrier injection problem, the dependency of the peak drain-source voltage of relevant transistors on the supply voltage during the transmit mode is compared in Fig. 3 (d). The conventional I/O buffer in Fig. 1 (a) reveals a peak voltage of MN0 as high as 2.96 V at 2.0-V supply voltage, suffering from severe hot-carrier injection. For the conventional buffer in Fig. 1 (b), the peak voltages of MN0, MN2, and MN3 reach up to 1.64 V. Meanwhile, the peak voltages of MN0 and MN2 in the proposed buffer are just up to 1.20 V, indicating up to 59.4% peak voltage reduction as compared to conventional I/O buffers.

5 Conclusion

In this paper, a low-voltage small-area mixed-voltage I/O buffer is proposed. The proposed I/O buffer provides lower latency at low supply voltages and has smaller layout area than conventional I/O buffers. The conventional and proposed mixed-voltage I/O buffers are designed in an 80-nm CMOS process, whose comparison results indicate that the proposed I/O buffer achieves 73% latency reduction, 23% operating voltage reduction, and 31% area reduction as compared to conventional I/O buffers.

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