A low voltage, high linear, and tunable triode transconductor

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Abstract: A low voltage, highly linear, and tunable triode transconductor is presented. The proposed transconductor uses a two-stage amplifier to regulate drain-source voltage of input devices. Thereby, high linearity can be achieved. The proposed design is able to operate at low supply voltage. The linear input range can be obtained up to 1.5 V at 1.8 V supply voltage. The simulated total harmonic distortion is $-61$ dB with 0.7 V\textsubscript{pp} input signal. The design uses TSMC 0.18 $\mu$m CMOS technology and supply voltage is 1.8 V. Simulation result shows that the tuning range of the proposed transconductor can be ranged from 220 $\mu$A/V to 869 $\mu$A/V.

Keywords: linear, tunable, low power, transconductor

Classification: Integrated circuits

References

1 Introduction

Transconductor is a fundamental building block in many analog and mixed-signal circuit applications, such as continuous-time filters and delta-sigma modulators. The function of transconductor is to convert input voltage into output current. The most critical design requirement is high linearity. Tuning ability of transconductor is also required in filter application which needs to adjust center frequency and quality factor of filter. In order to catch up with low-power consumption and low-supply voltage trend, it is necessary to develop new design technique which can meet circuit’s specification under crucial condition. In terms of designing low-voltage and highly linear transconductor, two issues need to be considered. The first issue is linear input range. Constant transconductance, $G_m$, is the critical parameter to determine input range. It decides the distortion in output currents for a given input voltage range. The second issue is control voltage that affects transconductance, linear range, and power consumption. As control voltage increases, transconductance increases at the penalty of decreased linear range and increased power consumption. Therefore, this issue is critical in low voltage applications. Besides, tuning range of control voltage also influences the performance and applications of transconductor. Several circuit design techniques to improve linearity of transconductors have been reported in literatures. The linearization methods include: source degeneration using resistors or MOS transistors, crossing-coupling of multiple differential pairs, class-AB configuration, adaptive biasing, and constant drain-source voltages [1, 2, 3, 4, 5, 6].

Conventional source degeneration using resistors or MOS transistors is the simplest method of linearization technique. The major drawback is that large resistor is needed in order to maintain a wide linear input range. The transconductor using crossing-coupling of multiple differential pairs is only suitable for balanced input signals. Class-AB configuration mainly focuses on low power consumption. However linearity is the worst due to the inherit Class-AB structure. Adaptive biasing technique produces a tail current that is proportional to the square of input differential voltage, but it is complicated to implement the square circuitry. The technique of using constant drain-source voltage is a simple structure that can achieve a better linearity. However, it needs to maintain $V_{DS}$ of input devices in low voltage such that these devices are in triode region. Hence, it is difficult to utilize this technique in low supply voltage application. In order to overcome the difficulty of using constant drain-source voltage in low voltage design, a low-voltage, highly linear, and large tuning range of MOS transconductor is proposed.

The paper is organized as follows. Section 2 discusses the linearization technique of using constant drain-source voltage. The proposed transconductor is presented in Section 3. The simulation results are shown in Section 4. Finally, conclusion is given in Section 4.
2 Transconductor using constant drain-source voltage

Transconductor using constant drain-source voltages is shown in Fig. 1. Assuming that transistors M₁ and M₂ are in triode region, M₃ and M₄ are in saturation region, and V_C is control voltage, considering perfectly matched M₁-M₂, M₃-M₄, and ignoring the channel length modulation effect, body effect, and other second-order effects, the drain current of M₁ and M₂ is given by

\[ I_D = \beta \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right] \]  

(1)

where \( \beta = \mu_n C_{ox} \frac{W}{L} \), \( V_{GS} \) is gate-to-source voltage, \( V_T \) is threshold voltage, and \( V_{DS} \) is drain-to-source voltage. If two amplifiers in Fig. 1 are ideal, we can obtain equation \( V_{DS1} = V_{DS2} = V_C \). The transfer characteristic of this transconductor is given by

\[ I_{out} = I_{out1} - I_{out2} = \beta V_C (V_1 - V_2) \]  

(2)

Transconductance value can be derived as

\[ G_m = \beta V_C \]  

(3)

Although this linear technique has a simple structure to achieve better linearity, it still has some restrictions. First, since both M₁ and M₂ are operating in triode region, \( V_{DS} \) must be small enough to keep transistors of input devices in triode region. Second, control voltage \( V_C \) must be carefully controlled to keep \( V_{DS1} = V_{DS2} = V_{DS} \). In next section, a new method to improve the constant drain-source voltage design is proposed.

3 The proposed transconductor

Since conventional structure of regulated cascode (RGC) with NMOS [6] or PMOS [7] can not operate at lower supply voltage, a triode transconductor
design is proposed by replacing the auxiliary amplifier in Fig. 1 with a two stage amplifier. This amplifier is composed of MOS transistor \( M_5, M_7, M_9, \) and \( M_{11} \) as shown in Fig. 2. The two-stage amplifier is implemented by using \( M_9 \) with active loads \( M_{11} \) as first stage and \( M_5 \) with active load \( M_7 \) as second stage. In order to maintain the stability of amplifier, a RC compensation circuit is placed between first and second stages of amplifier. The circuit of the proposed transconductor is shown in Fig. 2. The overall gain of two stage amplifier is given in following equation.

\[
A_v = A_1 \times A_2 = \frac{g_{m9} (r_{O9} \parallel r_{O11}) g_{m5} (r_{O5} \parallel r_{O7})}{1 + g_{m9} (r_{O1} \parallel r_{O3})} \tag{4}
\]

![Fig. 2. Whole circuit of the proposed transconductor](image)

Assuming that overall gain is large enough to keep transistors \( M_1 \) and \( M_2 \) in triode region, the transfer characteristic can be derived as

\[
I_{out} = I_{out1} - I_{out2} = \beta_1 V_{DS1} (V_{in1} - V_{in2}) \tag{5}
\]

where \( \beta_1 = \beta_2, \ V_{T1} = V_{T2}, \) and \( V_{DS1} = V_{DS2}. \) MOS \( M_9 \) is in saturation region, \( V_{DS1} \) can be found in (6)

\[
I_9 = \frac{1}{2} \beta_9 (V_{GS9} - V_{T9})^2 \Rightarrow V_{GS9} = \sqrt{\frac{2I_9}{\beta_9}} + V_{T9} \Rightarrow V_C - V_{DS1} = \sqrt{\frac{2I_9}{\beta_9}} + V_{T9}
\]

\[
V_{DS1} = V_C - \sqrt{\frac{2I_9}{\beta_9}} - V_{T9} \tag{6}
\]

According to (5)

\[
I_{out} = \beta_1 V_{DS1} (V_{in1} - V_{in2}) = \beta_1 \left( V_C - \sqrt{\frac{2I_9}{\beta_9}} - V_{T9} \right) (V_{in1} - V_{in2})
\]

Thus the transconductance \( G_m \) can be expressed as

\[
G_m = \beta_1 \left( V_C - \sqrt{\frac{2I_9}{\beta_9}} - V_{T9} \right) \tag{7}
\]

From (7), the transconductance can be tuned by controlling voltage \( V_C \) and current source \( I_9. \) To keep \( M_1 \) and \( M_2 \) in triode region, the following inequality \( V_{DS1} < V_{GS1} - V_{T1} \) needs to be satisfied. From (6)

\[
V_C - \sqrt{\frac{2I_9}{\beta_9}} - V_{T9} \leq V_{GS1} - V_{T1} \Rightarrow V_C \leq V_{GS1} + \sqrt{\frac{2I_9}{\beta_9}} - (V_{T1} - V_{T9}) \tag{8}
\]
To prevent $M_9$ entering cut-off region, the following relation (9) needs to be satisfied.

$$V_{DS1} + V_{T9} \leq V_C$$  (9)

According to (8) and (9), the linear range which $V_C$ can be tuned is shown in (10).

$$V_{DS1} + V_{T9} \leq V_C \leq V_{GS1} + \sqrt{\frac{2I_9}{\beta_9}} - (V_{T1} - V_{T9})$$  (10)

In order to achieve wide linear input range the supply voltage of the proposed transconductor is chosen as 1.8 V. Moreover, $M_9$ is needed to obtain negative feedback to keep drain-source voltage of $M_1$ constant. The control voltage $V_C$ is set between 0.65 V~0.78 V. Hence, wide tuning range can be achieved and used for different applications. In addition, the proposed transconductor has a simple structure and thus saves the cost in chip area. The output signal of Common Mode Feed Back (CMFB) amplifier connects to main transconductor and adjusts DC current of output stage as shown in Fig. 2. Hence, output DC level can be maintained at a constant level.

4 Simulation Results

The proposed design is simulated with TSMC 0.18 $\mu$m CMOS technology. The supply voltage is 1.8 V. The error of transconductance in the proposed design is less than 1% within ±0.75 V input voltage. Therefore, input linear range is up to 1.5 V. The simulated transfer characteristic with different control voltages ($V_C$) is shown in Fig. 3 (a). When $V_C$ is set between 0.65 V and 0.78 V, linear input range can be up to 1.5 V and transconductance error is less than 1%. The smallest transconductance and power dissipation are 220 $\mu$A/V and 0.743 uW when $V_C$ is 0.65 V. The highest transconductance and power dissipation are 869 $\mu$A/V and 1.768 uW when $V_C$ is 0.78 V. Therefore, the proposed transconductor is capable of achieving wide tuning range. The simulated Total Harmonic Distortion (THD) as a function of input frequency vs. amplitude of input signal is plotted in Fig. 3 (b). The THD of the proposed transconductor achieves less than $-61$ dB for 0.7 V pp (peak-to-peak) at 1 MHz.

5 Conclusions

A low-voltage triode transconductor with high linearity and tuning ability is presented. The proposed design can operate at low supply voltage by composing of a two-stage amplifier that regulates the $V_{DS}$ of input devices. Thereby, high linearity can be achieved. The proposed transconductor achieve wider tuning range with comparable THD performance. The input range of the proposed transconductor can be up to 1.5 V at 1.8 V supply voltage and THD is $-61$ dB for 0.7 V pp input signal at operation frequency of 1 MHz. The design uses TSMC 0.18 $\mu$m CMOS technology. It possesses wide tuning range of transconductance from 220 $\mu$A/V to 869 $\mu$A/V while it still maintains wide linear input range.
Fig. 3. (a) Transconductance for different values of control voltage (b) Simulated THD for different input frequencies

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