A compact Verilog-A model for Multi-Level-Cell Phase-change RAMs

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Abstract: A new compact but accurate Verilog-A model for Multi-Level-Cell Phase-change RAMs is proposed in this paper. The previous circuit-based SPICE macromodel has to have a very complicated circuit to describe multi-level resistance thus it needs a long simulation time and occupies large computer memories. This new Verilog-A model can easily model the multi-level resistance by using the partial SET and RESET states where PCRAM resistance changes continuously without having a complicated circuit-based macromodel. Moreover, this new model is more portable, reliable, and simpler than the traditional C-based SPICE model owing to the advantage of Verilog-A. The new model has been compared with the measurement and proved to have good agreement with the measurement.

Keywords: Phase Change RAMs, Verilog-A model, macromodel, Multi Level Cell, resistive memories

Classification: Integrated circuits

References


1 Introduction

Resistive switching memories such as Phase-Change RAMs (PCRAMs) have been developed due to their potential possibility to replace current DRAMs and Flash memories that are struggling with various kinds of scaling issue [1]. To push these resistance memories more forward in terms of memory density, Multi-Level-Cell (MLC) PCRAMs have also been considered recently [2]. Unlike Single-Level-Cell (SLC) PCRAMs having only SET and RESET states, MLC PCRAMs can have many different states by changing their cell resistance according to varying the pulse width and amplitude of the programming current thus being able to increase its memory density more without advancing its process technology.

Some MLC PCRAMs have been successfully demonstrated thereby its circuit applications being more demanded [2]. To develop the MLC PCRAM circuits, an accurate but compact MLC PCRAM model is needed in its circuit-level simulation.

To develop a new MLC PCRAM model, we need to review the previous models. The previous models of resistance memories can be divided into two types. One is the circuit-based macromodels that describe the behavior of their resistance switching by using circuit elements such as OP amps, resistors, capacitors, switches, and so on [3, 4] and the other approach is the Verilog-A model which is based on the hardware description language and can model the analog characteristics of resistive switching memories accurately by using a kind of computer language [5, 6]. The macromodel approach needs a lot of circuit elements to describe MLC operation [3, 4]. Figure 1 (a) shows a cross-sectional view of a typical PCRAM cell that consists of the anode, the cathode, and the resistance switching material between them. Figure 1 (b) illustrates an example of the MLC macromodel [4] that has 6 different SET resistance values. As you can see in Figure 1 (b), it is modeled by a very complicated circuit which occupies large computer memories and need a long simulation time. In addition, the resistance of the MLC PCRAM macromodel can’t be continuously changing with varying the state variable as shown in Figure 1 (c). Instead, the PCRAM resistance of the macromodel has discrete values in Figure 1 (c) that increases inaccuracy of the circuit simulation that uses MLC PCRAMs. For the other approach based on the Verilog-A, the previous Verilog-A models are all for SLC PCRAMs [5, 6] and the MLC Verilog-A model has not been developed yet.

Based on the above discussions, we will propose a compact but accurate Verilog-A model for the MLC PCRAMs in this paper. Comparing the pre-
previous PCRAM Verilog-A models that describe only two states of the SET and RESET [3, 4], this new model has two more intermediate states of the partial SET and partial RESET, in addition to the full SET and full RESET. At the partial states, the MLC resistance can change continuously between the full SET and full RESET according to the state variable calculated. By doing so, this model can avoid any discrete and stepwise nature in the resistance vs. state variable curve that is inevitable in the circuit-based SPICE macromodel [3, 4], thereby implementing more accurate and physical model particularly in MLC applications. At the same time, this Verilog-A model is much more portable and simpler than the traditional C-language-based SPICE model thus being able to reduce its model-developing time signifi-
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The new Verilog-A model for MLC PCRAMs is based on the state diagram shown in Figure 1 (d). In the state diagram, we can see two more intermediate states of the partial SET and partial RESET where the resistance of PCRAM can change continuously between the full SET and full RESET resistance. Whereas, the full SET and full RESET states have fixed resistance values. At the full RESET or SET state, if any programming pulse is applied, the full SET or RESET state goes to its partial state. At the partial state, the MLC resistance can change continuously as a function of state variable. This continuously changing resistance during the partial state is very different from the previous circuit-based SPICE macromodel that describes the MLC resistance in the discrete and stepwise way as shown in Figure 1 (c) [3, 4].

This proposed Verilog-A model is simulated in the CADENCE SPICE and Figure 2 (a) shows its simulated current-voltage characteristics. If the state variable is calculated to be large enough to change its state, the full RESET or partial SET goes to the full SET with resetting the state variable.

![Figure 2](image)

**Fig. 2.** (a) Simulated current-voltage curves of MLC PCRAM with the full SET, partial SET, and full RESET states (b) The parameters used in the simulation of the proposed Verilog-A model of MLC PCRAM [5]
to zero, as shown in Figure 2 (a). The model parameters that come from [5] are shown in Figure 2 (b). According to the state variable calculated, the MLC resistance can vary from the full RESET as large as 200 KΩ to the full SET as small as 7 KΩ. When the programming current exceeds the $I_X$, the MLC has the $R_{ON}$. And, when the MLC voltage between the anode and cathode becomes larger than the $V_{TH}$, its current begins to decrease showing negative resistance region where the RESET resistance goes to the point of $(V_X, I_X)$, as shown in Figure 2 (a). As the partial SET advances more, the MLC resistance goes smaller and the negative resistance region becomes shorter. As the state variable reaches the full SET state, the MLC resistance becomes 7 KΩ when its current is smaller than $I_X$. If we increase the programming current larger than the $I_X$, the MLC resistance is decreased more to the $R_{ON}$ as low as 1 KΩ.

3 Comparison between the model and measurement

Figure 3 (a) shows comparison of the measurement and simulation of the MLC

![Comparison between the measurement and simulation of the MLC resistance](image)

![Crystal fraction ratio at the partial RESET and SET states](image)

![Waveform of the programming current pulses for writing the SET](image)

![Waveform of the MLC resistance varying from the full RESET to the SET via the partial SET state](image)

**Fig. 3.** (a) Comparison between the measurement [1, 5] and simulation of the MLC resistance at the partial SET and RESET states when the amplitude of the programming current is varied (b) Crystal fraction ratio at the partial RESET and SET states when the amplitude of the programming current is varied (c) Waveform of the programming current pulses for writing the SET (d) Waveform of the MLC resistance varying from the full RESET to the SET via the partial SET state
resistance during the partial SET and RESET state when the amplitude of the programming current pulse varies. Here the measurement data is obtained from [1, 5]. The MLC is initially at the RESET with 200 KΩ. As the current pulse amplitude becomes higher, the MLC resistance is decreasing more, moving toward the partial SET. When the amplitude reaches as high as 600 µA, the MLC finally goes to the full SET state and its resistance saturates around 7 KΩ. The MLC resistance at the partial SET can be calculated by [8]

\[ R_X = R_{SET} + (R_{RESET} - R_{SET}) \cdot (1 - C_X) \]  

(1)

where \( C_X = 1 - e^{-X/A(X)} \), \( A(X) = B \cdot e^{C/X} \), and \( X = \int I^2 \cdot R_{ON} dt \).

Here the \( R_X \), \( R_{RESET} \), and \( R_{SET} \) are the partial SET resistance, the full RESET resistance, and the full SET resistance, respectively. And, the \( X \) in the equation (1) is the state variable to calculate the crystal fraction ratio \( (C_X) \) and in this paper, is given by integrating power of the PCRAM resistance with respect to time. It has the same dimension with energy. Here it should be noted that the PCRAM resistance in the equation (1) is the \( R_{ON} \) in Table I when the SET and RESET current pulse (I) is applied, as shown in Figure 2 (a). One more thing to decide the crystal fraction ratio is the A(X). Here the A(X) function comes from the equation (5) in [8] and the fitting parameters (B and C) for the A(X) can be easily extracted from the measured PCRAM resistance to minimize error between the model and measurement. The B and C parameters of the partial SET are \( 3.9621 \times 10^{-12} \) and \(-3.0574 \times 10^{-14} \), respectively. The above equation (1) is the same with the equations (3), (4), and (5) in [8], assuming the whole energy caused from the current flowing through PCRAM is converted to temperature. The reason why we use the state variable (X) instead of using the time (t) unlike the equation (4) in [8] is to calculate thermal energy only when the RESET or SET current pulse is applied. The time integral is done by the embedded function in Verilog-A. Similarly, the resistance at the partial RESET state can be calculated by the same equation (1) and the results are also shown in Figure 3 (a). The B and C parameters for calculating the partial RESET resistance are 0.2889 and \(-2.662 \times 10^{-9} \), respectively. Here the amplitude of the current pulse changes from 700 µA to 1200 µA. In the case of 700 µA, the MLC resistance is raised very little from 7 KΩ, but, as the amplitude increases up to 1200 µA, the resistance goes up to almost 200 KΩ. Figure 3 (b) shows the crystal fraction ratios at both the partial SET and RESET which are calculated by the equation (1).

Figure 3 (c) demonstrates the waveform of the applied programming current pulse and Figure 3 (d) shows how the MLC resistance changes according to the applied current pulse. In Figure 3 (c), you can see that two sequential pulses of the programming current are repeating six times. In each two pulses, the first one is for writing the SET and the second is for returning the MLC to the RESET. The amplitude for the first pulse is incremental from 100 µA to 600 µA by as much as 100 µA to change the partial SET resistance. The amplitude of the second is fixed at 1200 µA only to return the MLC to
the full RESET having 200 KΩ.

4 Conclusions

In this paper, the new Verilog-A model for MLC PCRAMs was proposed. Unlike the previous circuit-based SPICE macromodels, this model can change its resistance continuously without showing any discrete and stepwise nature. And, the new Verilog-A model is more portable, reliable, and simpler than the traditional C-based SPICE model. The new model was compared with the measurement and was proved to have good agreement with the measurement.

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