Area-efficient digitally controlled CMOS feedback delay element with programmable duty cycle

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Abstract: A novel area-efficient on-chip feedback delay element (FDE) has been designed and evaluated in 0.18-μm CMOS technology. The circuit utilizes positive feedback to achieve both digitally controlled propagation delay and programmable duty cycle with only 9.5% silicon area of the conventional capacitor-loaded delay element (DE). The proposed FDE with monotonic delay step is suitable for use in area-sensitive and high-speed CMOS VLSI applications for memories and CPUs.

Keywords: delay element, propagation delay, delay circuit, duty cycle

Classification: Integrated circuits

References


1 Introduction

Digital delay elements (DEs) are widely used in many high-speed CMOS VLSI circuits design for CPUs and DRAMs. A single-ended digital DE is used to produce delayed output clock (or other pulse) signal by a certain amount of time. A typical delay line, which introduces a significant propa-
gation delay, is composed of a chain of digital DEs in series. Fig. 1 a and 1 b show the basic structure of typical digital DEs based on resistive-capacitive (RC) delay: Fig. 1 a is basically a CMOS inverter and the propagation delay depends on the size of the on-chip resistor (R) and/or capacitor (C_L) loads connected with switching transistors (M_s). Here the basic idea is to adjust the delay by controlling either analog voltages or digital input vectors to change the effective RC time constant (τ). The practical examples include current starved inverter, digitally adjustable resistor, and capacitor loaded inverter types [1, 2, 3, 4]. All of these conventional DEs require very large silicon area for diffusion or polysilicon R and MOS capacitor C_L loads, leading to larger area and parasitic capacitances as well as higher cost. In this Letter, we propose a novel digitally controlled, area-efficient, single-ended CMOS feedback delay element (FDE), shown in Fig. 1 c, to adjust the propagation delay as well as the duty cycle. Compared with the previously reported DEs [1, 2, 3, 4], two key advantages of the FDE are its smallest layout size and the duty correction capability. To achieve the same amount of delay, the required silicon area of the FDE is only about 9.5% of the conventional capacitor-loaded DE (Fig. 1 b). The proposed FDE is the first CMOS implementation that utilizes positive feedback for programmable on-chip delay and duty cycle control.

Fig. 1. Delay elements (a) Basic structure of typical DE based on RC loadings (b) Conventional capacitor-loaded 2-stage DE (c) Proposed 2-stage feedback delay element (FDE) (d) Proposed feedback delay control block with 3-bit digital inputs.

2 Circuit design

In the conventional capacitor-loaded 2-stage DE (Fig. 1 b), the delay can be increased by adding more capacitive loads, which must require very large silicon area for M_{L1} and M_{L2} in the delay control block. On the other hand, Fig. 1 c shows the proposed 2-stage FDE composed of two CMOS inverters (M_{n1} − M_{p1} and M_{n2} − M_{p2}) and a feedback delay control block.
(M_{F1} - M_{F2} - M_{s1} - M_{s2}), which occupies much less silicon area than that of the conventional capacitor-loaded 2-stage DE. When the two switch transistors (M_{s1} - M_{s2}) are turned on, the delay control block and the second inverter (M_{n2} - M_{p2}) together form a pair of cross-coupled inverters and hence generate a positive feedback in the circuit. As a result, there is a contention between the first inverter and the feedback delay control block when input level changes. The positive feedback and the contention are exploited to achieve both variable switching threshold, which is known as hysteresis in [5], that can generate intentional timing delay in the first inverter and sharp rising and falling edges of the output (Out) in the second inverter.

The operation of the proposed FDE (Fig. 1 c) can be described as follows. First suppose that the two switching transistors (M_{s1} - M_{s2}) are turned off (a0 = low and b0 = high). Then the FDE is just a two CMOS inverters in series with no feedback and the delay from In to Out is just two inverter delays. Ideally in this case, the switching threshold (V_{st}) of the first inverter is determined by the ratio of \(\frac{\beta_{p1}}{\beta_{n1}}\), where \(\beta_{p1} = \mu_p C_{ox}(W/L)_{M_{p1}}, \beta_{n1} = \mu_n C_{ox}(W/L)_{M_{n1}}\), where \(C_{ox}\) is the gate capacitance, \(W\) and \(L\) denote the width and length of each transistor, and \(\mu_p\) and \(\mu_n\) are the mobility of PMOS and NMOS, respectively. If \(\frac{\beta_{p1}}{\beta_{n1}} = 1\) and \(V_{tn} = -V_{tp}\), then \(V_{st} = V_{st0} = V_{dd}/2\), where \(V_{dd}\) is supply voltage, \(V_{tn}\) and \(V_{tp}\) are the threshold voltages. Second suppose that the two switches (M_{s1} - M_{s2}) are turned on and the input changes from low-to-high. Since the node Z is high and Out is low at the beginning, M_{F2} is turned on and M_{F1} is turned off. This enables a pull-up network (consisting of PMOS M_{p1} in parallel with the two series connected feedback transistors M_{F2} - M_{s2}) and a pull-down network (consisting of NMOS M_{n1}) on the node z. This moves the switching threshold voltage from \(V_{st0}\) to \(V_{st lh}\). Depending on the ratio of Eq. (1), \(V_{st lh}\) will be higher than \(V_{st0}\) if \(\frac{\beta_{p1} + \beta_{F2}}{\beta_{n1}} > 1\), where \(\beta_{p1}, \beta_{F2}, \beta_{n1}\) are defined by the transistors M_{p1}, M_{F2} - M_{s2}, and M_{n1}, respectively.

\[
\frac{\beta_{p1} + \beta_{F2}}{\beta_{n1}} > 1
\]

\[
\beta_{F2} = \frac{(\beta_{F2} + \beta_{s2})}{(\beta_{F2} + \beta_{s2})}
\]

During the required time of input rising from \(V_{st0}\) to \(V_{st lh}\), the falling signal on the node Z is delayed slightly in the time domain. Similarly, if the input changes from high-to-low, the rising signal on the node Z is also delayed. Fig. 1d illustrates a technique for implementing a feedback delay control block of the FDE with 3-bit digital inputs (a0~a3 and b0~b3). By digital programming of the feedback delay control block, the first inverter’s trip point can be shifted, depending on the direction of the input (In) transition, making it possible to achieve monotonically increased or decreased delay amount as well as variable duty cycle.

3 Experimental results

The conventional capacitor-loaded 2-stage DE (Fig. 1 b) and the proposed 2-stage FDE (Fig. 1 c) have been designed and evaluated in 0.18-μm CMOS
Fig. 2. (a) Transient response of the conventional capacitor loaded 2-stage DE (b) Transient response of the 2-stage FDE (c) Programmable duty cycle correction capability of the 2-stage FDE $M_{s1} = \text{OFF}$, $M_{s2} = \text{OFF}$ (d) $M_{s1} = \text{ON}$, $M_{s2} = \text{OFF}$ (e) $M_{s1} = \text{OFF}$, $M_{s2} = \text{ON}$ (f) $M_{s1} = \text{ON}$, $M_{s2} = \text{ON}$.

technology. It is assumed that each delay control block has 3-bit input vectors for programmable delay control. Fig. 2a and 2b show the HSPICE simulated transient behaviors of the above two circuits with input low-to-high transitions. Fig. 2c, 2d, 2e, and 2f describe the duty correction capability of the proposed FDE. In Fig. 2a, when the delay control block is fully turned off, the delay from 50% In to 50% Out is about 90 ps. The falling signal shape on the node Z has been distorted and degraded seriously as more input vector switches are turned on. The delay amount of the above two circuits with ascending 3-bit (from $[0 \ 0 \ 0] = 0$ to $[1 \ 1 \ 1] = 7$) input vectors are compared in Fig. 3a. As can be seen in Fig. 2a and Fig. 3a, the conventional DE shows non-monotonically increased delay amount from 90 to 215 ps with a non-regular delay step of around $7 \sim 63$ ps for each input vectors. This is because the input capacitance of the MOS capacitor loads is not linear through wide operating range and therefore the inverter propagation delay is not linear as well.

In Fig. 2b, the voltage signals of the proposed FDE are shown for the same 3-bit input vectors. When the delay control block is fully turned off, the delay from In to Out is about 82 ps, which is almost same as that of the above DE. However, unlike the above conventional DE, the signal shape on the node Z has not been distorted that much as more input vector switches are turned on. As can be seen in Fig. 2b and Fig. 3a, the FDE shows better signal integrity and relatively monotonic delay from 82 to 225 ps with a regular delay step of around $13 \sim 37$ ps. To compare the silicon layout size, the key transistor sizes ($M_{L1} - M_{L2}$ versus $M_{F1} - M_{F2}$) of each delay
Fig. 3. (a) Comparison of delay versus control block input setting (b) Delay control block layout size comparison with mirror ratio (m).

control block are illustrated in Fig. 3b. The two inverter sizes of the above DE (Fig. 1b) and the FDE (Fig. 1c) are same. The W/L size of $M_{F1}-M_{F2}$ of the FDE occupies an area of $3/0.25 (\mu m)$, $m = 16$ to achieve a delay of about 225 ps, where $m$ is the layout mirror ratio. This silicon area is only 9.5% of the $M_{L1}-M_{L2}$ size of the conventional DE (Fig. 1b) that occupies an area of $3/0.25 (\mu m)$, $m = 168$ for a delay of about 215 ps. The FDE consumes an average current of $0.3 \sim 1.2$ mA from a 1.8 V at 0.5 GHz, which is almost same as that of the conventional DE.

Unlike the conventional capacitor-loaded DE which is not able to adjust duty cycle, another advantage of the FDE is its duty cycle correction capability: As shown in Fig. 2d and 2e, conducting more pull-down networks ($M_{s1} = ON, M_{s2} = OFF$) of the delay control block increases the duty cycle of up to 60% and conducting more pull-up networks ($M_{s1} = OFF, M_{s2} = ON$) will decrease the duty cycle of up to 40%, resulting in a programmable duty correcting range of larger than $+/−10\%$ at 0.5 GHz. As shown in Fig. 2c and 2f, the duty cycle ratio will not be changed and remains in 50% if the pull-up ($M_{s2}$) and pull-down ($M_{s1}$) networks of Fig. 1c are evenly turned-off (Fig. 2c) and turned-on (Fig. 2f).

4 Conclusion

A novel technique for an area-efficient CMOS on-chip delay element has been described. Unlike the conventional capacitor-loaded DE based on RC delay, the proposed FDE circuit exploits using of positive feedback to achieve digitally adjustable propagation delay with monotonic time step. To achieve the same amount of delay, the required silicon area of the proposed 2-stage FDE is only 9.5% of the conventional capacitor-loaded 2-stage DE. The FDE also has a benefit of programmable duty cycle of larger than $+/−10\%$ at 0.5 GHz. This new on-chip CMOS delay element is suitable for use in area-sensitive high-speed VLSI design for memories and microprocessors.

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