TX rise/fall time control for multi-rate serial link

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Abstract: For a multi-rate serial link, the proposed TX rise/fall time (tTR) control scheme enables tTR to be changed according to data rate. The main driver is split into multiple legs and each leg is controlled by its own pre-driver. All pre-drivers are biased on for the smallest tTR while some pre-drivers are biased off for large tTR. Due to $RC$ delay among pre-drivers, the transition of a biased-off pre-driver’s output occurs later but becomes overlapped with those of adjacent pre-drivers’ outputs so that there is no stair-step waveform shown. The measurement results show that the driver has a sufficient tTR control range of around three times.

Keywords: rise time, rise/fall time, multi-rate, serial link, driver

Classification: Integrated circuits

References


1 Introduction

According to skew, coupling, mismatch, and other mode conversions which occur in high-speed differential output (TXP and TXN) of a transmitter (TX), common-mode noise is generated in TXP and TXN, thereby exciting electromagnetic interference (EMI). The slow transition of TX high-speed output is desirable for EMI reduction, but the signal quality will get worse at
a receiver (RX). Therefore, 0.2~0.4UI (unit interval) TX rise/fall time (tTR) is optimal for both signal quality and EMI reduction.

However, in multi-rate applications [1, 2] with wide operating range, one fixed tTR cannot cover all data rates because different tTR requirement is defined for each data rate. Therefore, tTR must be controlled according to the data rate. For example, in 6-Gbps data rate, 1×UI (one UI) is 1/6 G sec (~167 ps) and 0.3×UI is 0.3×1/6 G sec (=50 ps). But, in 3-Gbps data rate, 1×UI (one UI) is 1/3 G sec (~333 ps) and 0.3×UI is 0.3×1/3 G sec (=100 ps). In a 6-/3-Gbps dual-rate application, tTR must be able to be set to either 50 ps or 100 ps according to the operating data rate.

In this paper, we propose a tTR control scheme for a 6-/3-/1.5-Gbps multi-rate application. The next section of this paper describes detailed circuit design. Section 3 gives the experimental results. Section 4 concludes and summarizes this paper.

2 TX rise/fall time control

In a previous implementation [3] as shown in Fig. 1 (a), tTR of a main driver is expected to be controlled by adjusting the pre-driver’s load ($C_{PDL}$). With increased $C_{PDL}$, the rise/fall time of the main-driver’s inputs (DP and DN) can be increased. However, due to the high gain of the main driver, tTR is not sufficiently changed but almost fixed as shown in Fig. 1 (a). In other words, tTR is just a weak function of $C_{PDL}$. Another conventional design [4] used a variable delay line as shown in Fig. 1 (b). Each leg of the main driver is switched using taps from the delay line. However, since a serialized data goes through a delay line, the data could get distorted, thereby the operating...
frequency being limited. And, the delay time between adjacent taps may cause stair-step waveform on the main-driver’s output.

In the proposed design as shown in Fig. 2 (a), the main driver is split into multiple legs. And, the gate voltages (DP[0:4] and DN[0:4]) of the legs can be switched either sequentially or simultaneously. Although the total number of the legs is assumed as five, the total number can be any other value. DP[0] and DN[0] are a differential signal pair, DP[1] and DN[1] are another differential signal pair, and so on. For smallest tTR, all DP[0:4] (and DN[0:4]) are switched simultaneously. For large tTR, some of DP[0:4] are switched later as shown in Fig. 2 (b).

The biasing of each pre-driver is controlled by En as shown in Fig. 2 (c). En is one of En[0:4], as shown in Fig. 2 (a). For example, the pre-driver which generates DP[0] and DN[0] has En[0] as the bias-control signal. If En is set to ‘1’ (logically HIGH), the corresponding pre-driver is enabled. Then, the gate voltage of a NMOS transistor MN0 in the pre-driver is set to a bias voltage $bias$, thereby making MN0 work as a current source. And, since Enb is low, PMOS transistors MP0 and MP1 are turned on. The turn-on resistance of MP0 (or MP1) and a resistor $R_P$ determine the loading resistance of the pre-driver. Since the turn-on resistance of MP0 (or MP1) is designed to be smaller than the passive resistance $R_P$, the process, voltage, and temperature (PVT) variations of the loading resistance are lowered. In short, if En is set to ‘1’, the corresponding pre-driver acts as a driver or a buffer.

If En is set to ‘0’ (logically LOW), MN0 is turned off. MP0 and MP1 are also turned off. So, the corresponding pre-driver simply acts as loading

![Fig. 2. Proposed driver with TX rise/fall time control: (a) block diagram, (b) timing diagram, and (c) pre-driver circuit.](image-url)
capacitance but not a driver. Some resistors are connected among pre-drivers’ outputs as shown in Fig. 2(a). Due to these $RC$ delays among pre-drivers, the output of a biased-off pre-driver will respond later sequentially to increase $t_{TR}$. The $RC$ network also enables the transitions of adjacent pre-drivers’ outputs to be overlapped as shown in Fig. 2(c) so that there is no stair-step waveform shown on the main-driver’s output.

In order to control $t_{TR}$ according to the data rate, pre-driver bias control signals, $En[0:4]$ are adjusted. For the smallest $t_{TR}$, all pre-drivers are biased “on” with $En[0:4]$ set to “11111”. For large $t_{TR}$, some pre-drivers are biased “off” with some of $En[0:4]$ set to ‘0’. If $En[0:4]$ is set to “10101” or “10001,” $t_{TR}$ will be increased.

3 Experimental Results

A prototype chip with the proposed TX rise/fall time control scheme was designed in a 0.13-$\mu$m CMOS technology [5]. The power supply voltage is 1.2 V. Fig. 3 shows TX eye diagrams measured at 6-/3-/1.5-Gbps data rates. At each data rate, $t_{TR}$ is measured between 20% and 80% of the differential

![Fig. 3. TX eye diagrams measured at (a) 6-Gbps, (b) 3-Gbps, and (c) 1.5-Gbps data rates.](image-url)
signal.

In the 6-Gbps TX eye diagram shown in Fig. 3 (a), En is set to “11111” and TX eye shows tTR of 50.7 ps which corresponds to 0.3 × UI. The TX eye shows 3.0-ps RMS and 22.7-ps peak-to-peak jitter performance. In the 3-Gbps TX eye diagram shown in Fig. 3 (b), En is “10101,” tTR is 84 ps (0.25UI), and the TX eye shows 3.7-ps RMS and 23.3-ps peak-to-peak jitter. In the 1.5-Gbps TX eye diagram shown in Fig. 3 (c), En is “10001,” tTR is 150 ps (0.23UI) and measured jitter is 3.6-ps RMS and 26.7-ps peak-to-peak. Therefore, when the data rate is changed from 6 Gbps to 1.5 Gbps, the proposed TX rise/fall time control shows a sufficient control range of around three times while TX jitter becomes just slightly increased. And, the peak-to-peak differential amplitude of TX output voltage is larger than 500 mV.

4 Conclusion

For a multi-rate serial link, the proposed TX rise/fall time (tTR) control scheme enables tTR to be changed according to data rate. In the proposed design, the main driver is split into multiple legs and each leg is controlled by its own pre-driver. All pre-drivers are biased on for the smallest tTR while some pre-drivers are biased off for large tTR. Due to RC delays among pre-drivers, the outputs of biased-off pre-drivers respond later sequentially. The RC network also enables the transitions of adjacent pre-drivers’ outputs to be overlapped so that there is no stair-step waveform shown on the main-driver’s output. The measurement results show that the driver has a sufficient tTR control range of around three times while TX jitter becomes just slightly increased.