ESD protection circuit with low triggering voltage and fast turn-on using substrate-triggered technique

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Abstract: In this paper, ESD protection circuit with substrate-triggered technique using PNP bipolar transistor for quick discharge of the electrostatic energy is proposed. The proposed ESD protection circuit is verified by the transmission line pulse (TLP) system. The results show that the proposed ESD protection circuit has lower trigger voltage (5.98 V) compared with that of conventional GGNMOS. And the proposed circuit has faster turn-on time (\textasciitilde37 ns) than that of the conventional substrate-triggered ESD protection circuit.

Keywords: ESD, gate grounded NMOS (GGNMOS), Turn on speed

Classification: Electron devices, circuits, and systems

References

1 Introduction

Electrostatic discharge has been considered as a major reliability threat in the semiconductor industry for decades. It was reported that ESD and EOS are responsible for up to 70% of failures in IC technology [1]. Therefore, each I/O must be designed with a protection circuitry that creates a discharge path for ESD current. As CMOS technology scales down, the design of ESD protection circuits becomes more challenging. This is due to thinner gate oxides and shallower junction depths in advanced technologies. A multi-finger gated grounded NMOS (GGNMOS) is the most widely used ESD protection circuit because of its active discharge mechanism and compatibility to CMOS technologies. Sometimes the multi-fingers GGNMOS cannot be uniformly turned on during ESD stress. Only several fingers of GGNMOS are turned on and this often causes a low ESD level. The substrate-triggered technique [2, 3, 4] is a useful method to reduce the trigger voltage. However, ESD protection circuits using these methods are not effective for fast turn-on.

In this paper, ESD protection circuits with substrate-triggered technique using a PNP bipolar transistor is proposed for lower trigger voltage and fast turn-on speed. This work has been successfully verified in foundry’s 0.13 um CMOS process.

2 Proposed ESD Protection Circuit

The substrate trigger technique is used widely to reduce the trigger voltage and to enhance turn-on uniformity of GGNMOS. Fig. 1 (a) shows conventional substrate-triggered NMOS [5] using PMOS (GGNMOS_PMONS). However, the conventional method has two problems due to the use of PMOS. The first problem is that the trigger PMOS (MP1) with a long channel length which reduces gate leakage slows turn-on time. The second is that the gate oxide of the trigger PMOS can be easily broken down by ESD surge. These problems are solved by using PNP bipolar transistors instead of trigger PMOS as shown in Fig. 1 (b).

Fig. 1. (a) Conventional Substrate-triggered NMOS using PMOS (GGNMOS_PMONS). (b) Proposed substrate-triggered NMOS using PNP bipolar transistor (GGNMOS_PNP).
Under normal operating conditions, the gate and substrate voltage of the NMOS (MN1) are zero and the NMOS is turned off. Therefore the protection circuit will not interfere with the normal functions of the input circuits.

When a positive ESD voltage is zapping on the pad with grounded, the ESD voltage can trigger the PNP (Q\textsubscript{PNP}) bipolar transistor into avalanche breakdown. Therefore, a substrate current generated by PNP bipolar transistor will flow into the base of the parasitic bipolar transistor (Q1) in the GGNMOS. It helps to forward bias base-emitter junction of the parasitic bipolar transistor. As a result, the triggering voltage is reduced and the turn-on uniformity of multi-finger GGNMOS is enhanced. Also, the use of PNP bipolar transistor with short base width can speed up the turn-on time which was the weak point of trigger PMOS with a long channel length.

3 Experimental results

3.1 TLP measurement

The I-V characteristic and DC-leakage current has been measured with a transmission line pulse (TLP) tester with a pulse duration of 100 ns, rising time of 10 ns. Figure 2 shows the TLP I–V curves of the conventional GGNMOS, GGNMOS\_PMOS, and GGNMOS\_PNP circuits having the same areas (a width of 400 \(\mu\)m). While GGNMOS has high trigger voltage of 9.92 V, each

![Fig. 2. Measured TLP I–V characteristics of conventional GGNMOS, GGNMOS\_PMOS, and GGNMOS\_PNP.](image-url)
circuit with substrate-triggered technique has low trigger voltage about 6 V. This result is very important for effective ESD protection circuit design. For the CMOS 0.13 \textmu m process, the target design window can be determined between the operating voltage of 3.3 V and the oxide breakdown voltage of 10 V. Although ESD protection circuits have high robustness, the effective robustness is limited by the design window. In the result, the robustness of GGNMOS\_PNP (1.71 A) is higher than that of conventional GGNMOS (1.4 A).

### 3.2 Turn-on Speed

The measured voltage waveform of the input signal on the pad with the proposed substrate-trigger NMOS using PNP bipolar transistor under normal operating condition is shown in Fig. 3 (a). The voltage waveform has no degradation when a 3.3 V voltage signal is applied to the pad. The experi-

![Fig. 3.](image)

(a) Measured voltage waveform of input signal on the pad with the GGNMOS\_PNP under normal circuit operating conditions. (b) Experimental setup to measure the turn-on speed. (c) Turn-on waveform of GGNMOS\_PMOS and GGNMOS\_PNP.
Table I. Comparison on the ESD characteristics between GGNMOS, GGNMOS_PMOS, and GGNMOS_PNP.

<table>
<thead>
<tr>
<th></th>
<th>$V_{th}$ (V)</th>
<th>$V_{th}$ (V)</th>
<th>$V_{G}$ (V)</th>
<th>Effective robustness (A) @ 10V</th>
<th>$I_{sat}$ @3.6V</th>
<th>Turn-on Time (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GGNMOS</td>
<td>9.92</td>
<td>6.58</td>
<td>14.52</td>
<td>1.4</td>
<td>100</td>
<td>-</td>
</tr>
<tr>
<td>GGNMOS_PMOS</td>
<td>5.95</td>
<td>5.91</td>
<td>10.58</td>
<td>1.68</td>
<td>130</td>
<td>~80</td>
</tr>
<tr>
<td>GGNMOS_PNP</td>
<td>5.98</td>
<td>5.71</td>
<td>10.54</td>
<td>1.71</td>
<td>80</td>
<td>~37</td>
</tr>
</tbody>
</table>

Experimental setup to measure the turn-on speed of ESD protection circuit under transient conditions is shown in Fig. 3 (b). The comparisons of turn on speeds between the GGNMOS_PMOS and the GGNMOS_PNP under 0-10 V voltage pulse with the pulse rising times of 25 ns are shown in Fig. 3 (c). The turn-on time of the GGNMOS_PNP (∼37 ns) is faster than that of the GGNMOS_PMOS (∼80 ns) under 0-10 V voltage pulse. From the experimental results, the GGNMOS_PNP is more suitable than the GGNMOS_PMOS for quick discharge of the electrostatic energy. The summary of comparison on the ESD characteristics is presented in Table I.

4 Conclusion

In this paper, for lower trigger voltage and faster turn-on speed ESD protection circuit with substrate trigger technique using PNP bipolar transistor is proposed. The proposed substrate-triggered ESD protection circuit has been verified in 0.13 um CMOS process. Compared to the conventional GGNMOS, the proposed circuit can provide much lower trigger voltage (5.98 V). And it shows faster turn-on time (37 ns) than that of the conventional substrate-triggered ESD protection circuit (∼80 ns). In the future, the proposed structures can be used for the output pad or power clamp circuit to further improve ESD robustness and turn-on speed in the deep-submicron process.

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