SSCG with Hershey-Kiss modulation profile using Dual Sigma-Delta modulators

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Abstract: This letter describes a spread spectrum clock generator (SSCG) circuit with the Hershey-Kiss modulation profile using two stacked sigma-delta modulators. The proposed Hershey-Kiss profile modulator generates various slopes to achieve non-linear modulation profile. Since the modulators are implemented by digital blocks, it can be modified for other applications. Simulation results show that peak power reduction level of 10.2 dBm with 5000 ppm down spreading at the 340 MHz operation using 0.13 μ m CMOS.

Keywords: spread-spectrum clock generator (SSCG), Hershey-Kiss profile, sigma-delta modulator, fractional-N PLL

Classification: Integrated circuits

References

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1 Introduction

As the operation frequency of electronic devices increases, the electromagnetic interference (EMI) has been generated and radiated to other devices. The spread spectrum clock generator (SSCG) is a PLL-based clock generator with an output frequency modulation to reduce the EMI. Amount of EMI reduction frequency varies on modulation profiles [1]. The linear modulation

known as the triangular profile is commonly used because of its simplicity for implementation. With the triangular modulation profile, however, most of the harmonic energy is concentrated at the edges of the spectrum distribution. On the other hand, the Hershey-Kiss profile has non-linear slope change and generates a more uniform spectral spreading. Therefore a better EMI peak reduction could be achieved. Conventionally the Hershey-Kiss profile modulator is implemented by the read only memory (ROM), which results in a large chip area [2]. This letter proposed a SSCG that generates Hershey-Kiss modulation profile using dual sigma-delta modulators. Since the proposed modulator is based on the digital blocks, it can be implemented in a small area and easily modified to other applications and specifications.

2 Concept of the proposed SSCG

Fig. 1 (a) shows a Hershey-Kiss modulation profile (top) and its slope change (bottom) of the modulation profile. Though the Hershey-Kiss modulation profile is non-linear, the variation of its slope can be approximated and it has a periodicity as shown in the bottom of Fig. 1 (a). Therefore the Hershey-Kiss profile can be generated by modulating its slope variation. Fig. 1 (b) illustrates the block diagram of the proposed PLL-based SSCG. The cascaded sigma-delta modulator block consists of a division modulator and a slope modulator. The slope modulator generates approximate slope values of the Hershey-Kiss profile. The division modulator produces sigma-delta modulated output by taking the sigma-delta modulated slope values. Therefore the final output of the cascaded sigma-delta modulators is provided to the multi-modulus divider, from which the PLL has a non-linear modulation profile on the VCO control voltage and the output clock is spectrum-spread.

Fig. 1. Profile and proposed SSCG block diagram
(a) Hershey-Kiss profile (top) and its slope change (bottom)
(b) Proposed SSCG block diagram

3 Architecture and operation

Fig. 2 shows a detailed block diagram of the proposed SSCG. The key blocks are a slope modulator, a division modulator and a fractional-N type PLL. The slope modulator generates various slope values for a Hersey-Kiss profile and the division modulator produces the sigma-delta modulated output for the multi-modulus divider in the PLL loop. As a result, the PLL has a Hershey-Kiss modulation profile on the VCO control voltage and the output clock is spectrum-spread.

Fig. 2. Block diagram of the proposed SSCG

3.1 Slope modulator

The slope modulator block has a 1st order sigma-delta modulator and an 8 bit up/down counter. The slope modulator generates the mode and the sign signal controlling the division modulator block for producing various slope values. The modulator used in the block is a 1st order sigma-delta modulator for monotonic increment or decrement of the slope [3]. The 1st order sigma-delta modulator transforms the 8 bit counter output into the one bit mode signal. The average value of the mode signal is assigned to the 8 bit counter output value. As the counter output is changed, the piecewise average of the mode signal is changed. The average value of the mode signal is the same as the absolute value of the slope. The average mode signal value (AMS) is given as

$$AMS = \frac{\text{output_of_Counter_1}}{2^{\text{Counter_1 bit size}}} \quad (1)$$

When the 8 bit up/down counter is used, the slope resolution is the 2^{-8} .

When SSCG operates, the counter in the slope modulator repetitively sweeps the output between the ‘K’ and 0. The ‘K’ is the largest number of the counter (counter_1) output. Whenever the output value reaches at ‘K’, the sign signal switches its value from 0 to 1 or from 1 to 0. The counter output represents the absolute value of the profile slope and the sign signal indicates the sign of the slope. The slope value change has a triangular profile as shown in Fig. 1 (a). The period of slope curve is a half of the Hershey-Kiss modulation period. So the modulation frequency (f_m) can be determined by the reference clock frequency and the ‘K’ value as given in Eq. (2).

$$f_m = \frac{\text{ref_CLK freq.}}{4 \times K} \quad (2)$$

3.2 Division modulator

As shown in Fig. 2, the division modulator block consists of a 2nd order sigma-delta modulator and a 14 bit up/down counter. The division modulator block generates the divider value for the PLL. The increment or the decrement of the count value is decided by the sign signal from the slope modulator. When the sign signal is ‘1’, the counter counts up and when the sign signal is ‘0’, the counter counts down. Since the step value of the counter is set as α or β ($\beta > \alpha$), the slope variation is either α or β . When the mode signal from the slope modulator is low, the counter value is increased or decreased by α . When the mode signal is high, the value of the data is increased or decreased by β . As a result, the slope variation is related to the average mode signal value (AMS), α , and β value. The slope of the Hershey-Kiss profile can be expressed as

$$\text{Slope of profile} = (\beta - \alpha) \times \text{AMS} + \alpha \quad (3)$$

Number of slope variation steps and their values can be varied based on applications and design specifications. In this letter, α and β are set to 1 and 3, respectively. When the K is 240₍₁₀₎, the steepest slope is 2.875. Thus the slope varies between 1 and 2.875. The spread ratio is controlled by the multi-modulus divider and the counter_2. The spread ratio can be derived as

$$\text{Spread ratio} = \frac{C_{2_max} - C_{2_min}}{N \cdot 2^{Counter_2 \text{ bit size}} + C_{2_max}} \quad (4)$$

N is the division ratio on the multi-modulus divider. C_{2_max} and C_{2_min} are the maximum and minimum number of the counter_2. The values of N , C_{2_max} , and the C_{2_min} can be determined by considering the reference clock, the target frequency and the spread ratio. In this letter, N , C_{2_max} and C_{2_min} are set as 11, 5461₍₁₀₎ and 4532₍₁₀₎, respectively, for a spread ratio of 5000 ppm.

4 Simulation results

The proposed SSCG has been designed using CMOS 0.13um process. Fig. 3(a) shows the simulated the Hershey-Kiss modulation profile of the proposed SSCG. The frequency of modulation profile is 31.25 KHz with a

Fig. 3. Simulated waveforms

(a) Hershey-Kiss modulation profile (b) Spectrum of non-SSC (c) Spectrum of SSC

5000 ppm spread ratio. The non-linear profile that has two different slope regions in near of the peak and in the middle range can be seen. Fig. 3 (b) is the spectrum of single 340 MHz tone clock in the non-SSC mode and Fig. 3 (c) shows the spectrum of the modulated output clock with the proposed profile. Comparing with the non-SSC PLL, the power reduction is about 10.2 dBm with 5000 ppm down spread ratio.

5 Conclusion

A spread spectrum clock generator (SSCG) circuit with Hershey-Kiss modulation profile is proposed. The proposed Hershey-Kiss profile modulator has two stacked sigma-delta modulators. Since the modulators are implemented by digital blocks, it can be modified for other applications and specifications. Simulation results show that peak power reduction level of 10.2 dBm with 5000 ppm down spreading at the 340 MHz operation using 0.13 m CMOS.

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