A 5.7 GHz low noise figure ultra high gain CMOS LNA with inter stage technique

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Abstract: A 5.7 GHz low noise ultra high gain CMOS LNA with inter stage technique is presented in this paper. The noise and gain performance is improved using common-source transistor inter stage network. A bias resistor of large value is placed between source and the body node to prevent body effect and reduce noise. The simulated 0.18 μm CMOS LNA achieves -14 dB and -17.5 dB input and output return loss respectively. Compared to previously published current-reused LNA, the proposed LNA has the smallest noise figure of 1.85 dB, extremely high gain 32.5 dB, and the highest Figure of Merit of 87.28.

Keywords: current-reuse, inter stage network, low noise amplifier, low noise figure, ultra high gain

Classification: Integrated circuits

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1 Introduction

Silicon based CMOS technology has become a competitive technology for rapidly-developing wireless broadband communications due to its low-cost, high-level integration of radio transceiver with base-band processors. The low noise amplifier is one of the key components in an RF receiver front-end because of its dominant noise contribution to the whole radio receiver noise. The design of LNA involves numerous aspects of requirements, including noise figure, gain, linearity, input/output matching and power consumption. A number of LNA topologies [1, 2, 3, 4, 5], such as the cascaded, the cascode, and the *gm*-boosted topologies, have been proposed to achieve the highest performance. Among the variety of topologies, the current-reused topology shows the most promising solution [1, 2, 3, 4].

The current-reused topology is basically composed of two stages of common source MOSFET transistors, in which the bias current is shared by these transistors such that the power consumption is only half of the cascaded topology. The RF signal is amplified by the first and the second CS transistors such that the power gain is as high as the cascade topology. The crucial design point in the current-reused topology is the inter-stage network, which directs the RF signal and simultaneously allows the same DC current flowing through two transistors. In other words, the inter-stage network plays dual functions of RF impedance matching and DC bias with RF choking effect.

In this paper, an enhanced current-reused topology using the common-source transistor inter-stage network is presented. New Topology discussed below which overcomes the drawbacks of the previous current-reused LNAs, is shown to have an extremely high gain, low noise figure and high FOM. The rest of paper is organized in the following way. The LNA circuit design details are discussed in Section II. Simulation results and conclusion will be studied in sections III and IV respectively.

2 Circuit design

The interface between the antenna and the LNA entails an interesting issue that divides analog designers and microwave engineers. Considering the LNA as a voltage amplifier, it is expected that the ideal value of its input impedance is infinite. From the noise point of view, a transformation network to precede the LNA to obtain minimum NF might be required. From signal power approach, conjugate matching between the antenna and the LNA may

be utilized. While each of these choices has certain advantages and drawbacks, the latter is dominant in today's systems, i.e., the LNA is designed to have a $50\ \Omega$ resistive input impedance [1].

2.1 Input matching

The proposed CMOS LNA is shown in Fig. 1 (a). The best method to present resistive input impedance is to employ a passive source degeneration component, while it is not a thermal noise generator.

(a)

(b)

Fig. 1. (a) Schematic of the proposed LNA. (b) Small-signal equivalent circuit of the LNA input stage with noise current sources.

In this circuit, L_g is chosen as $50/\omega_T$, while ω_T is unit gain frequency and L_g remains as a free parameter to provide a zero imaginary part at the desired frequency. Neglecting the gate drain capacitances, the input impedance of

the LNA shown in Fig. 1 (a) is:

$$Z_{in} = sL_g + sL_s + \frac{g_{m1}}{C_{gs1}}L_s + \frac{1}{sC_{gs1}}. \quad (1)$$

Where g_m , and C_{gs} are the transconductance and gate-source capacitance of the input transistor M_1 , respectively. As can be seen from (1), the source degeneration generates the real part at the input impedance. As can be seen in (1), Z_{in} has the imaginary part, after degeneration the real part would be negligible. Otherwise, there would be no real part in Z_{in} . Although not excessively, L_s helps to reduce the discrepancy between the real parts of Z_{opt} and Z_{in} of the LNA. By carefully selecting L_s , L_g and size of M_1 , the Z_{in} can be made equal to the input source resistance R_s which is 50Ω . Real valued impedance (typically 50Ω) by choosing L_s such that:

$$L_s = \frac{C_{gs}R_{in}}{g_m}. \quad (2)$$

And L_g such that:

$$(L_g + L_s)C_{gs}\omega^2 = 1. \quad (3)$$

2.2 Proposed inter stage architecture

The inter stage configuration can be considered as a three stage cascade amplifier, where the first and second stages are the CS amplifiers (M_1 , M_3), and the third stage is the cascode amplifier (M_2 and M_4). Note that M_4 is the common-gate stage of the cascode configuration, which eliminates Miller effect and provides a better isolation from the output return signal. The signal amplified by M_1 is coupled to the gate of M_3 and again amplified by M_3 is coupled to the gate of M_2 while the source of M_2 is bypassed by C_b . The circuit thus saves power through the reuse of the bias current. A simple L-C network using an on-chip inductor L_o and an on-chip capacitor C_o are used to implement the output matching network.

The transfer function of the third and second stage can be expressed as (4) and (5),

$$\frac{v_{out}}{v_{g2}} = g_{m2} \left((g_{m4}r_{o4}r_{o2}) || sL_o || \frac{1}{sC_{out}} \right). \quad (4)$$

$$\frac{v_{g2}}{v_{d1}} = g_{m3} \left(r_{o3} || sL_3 || \frac{1}{sC_{total3}} \right). \quad (5)$$

Where r_{oi} , C_{out} and C_{totali} are drain-source resistor of M_i transistor, total output capacitance and total capacitance of node i in circuit respectively. And finally, by neglecting r_{o1} , we have,

$$\frac{v_{d1}}{v_{in}} = \frac{\omega_T}{\omega_O} \frac{1}{R_{in}} \left(sL_1 || \frac{1}{sC_{total1}} \right). \quad (6)$$

2.3 Noise figure

One of important specification of the LNAs is the noise figure which is strongly influenced by input stage design. For a cascode topology with source degeneration, noise and power matching can be achieved simultaneously. To

have a better understanding on the input matching, the equivalent circuit utilized for noise analysis is shown in Fig. 1 (b), where v_{ns} and Z_{ns} are the Thevenin's equivalent of the source, and i_{ng}^2 and i_{nd}^2 represent mean-square values of the gate-induced and channel noise currents, respectively. Conventionally, the noise currents of a MOSFET are given by [6].

$$i_{ng}^2 = 4KT\delta g_g \Delta f. \quad (7)$$

$$i_{nd}^2 = 4KT\gamma g_{d0} \Delta f. \quad (8)$$

In the CMOS expressions, γ is the coefficient of channel thermal noise, Δf is the bandwidth, respectively. For long-channel devices, δ and γ have typical values of 4/3 and 2/3, respectively. It is noted that g_g can be expressed as (9),

$$g_g = \frac{\omega^2 C_{gs1}^2}{5g_{d0}}. \quad (9)$$

And g_{d0} is the zero-bias drain conductance. Assuming that the effect of g_{ds1} is negligible, the noise parameters of the two port equivalent circuit can be derived. The noise resistance R_n , the minimum noise factor F_{min} and the optimum source impedance Z_{opt1} are given by (10), (11) and (12) respectively.

$$R_n = \frac{\gamma}{\alpha} \frac{1}{g_{m1}}. \quad (10)$$

$$F_{min} = 1 + \frac{2\omega}{\sqrt{5}\omega_T} \sqrt{\gamma\delta(1 - |C|^2)}. \quad (11)$$

$$Z_{Opt,1} = j \frac{1}{\omega C_{gs1}} - j\omega L_S + \frac{\sqrt{\frac{\alpha^2\delta}{5\gamma}(1 - |C|^2)}}{\omega C_{gs1} \left[\frac{\alpha^2\delta}{5\gamma}(1 - |C|^2) + \left(1 + \frac{\alpha^2\delta|C|^2}{5\gamma}\right)^2 \right]}. \quad (12)$$

Where $\alpha = g_{m1}/g_{d0}$ and $|C|$ is a correlation coefficient with a predicted value of 0.395 [6]. Based on the small-signal analysis, the input impedance Z_{in1} at the gate of M_1 is approximated by (1).

From (1) and (12), the simultaneous power and noise matching is achieved if Z_{Opt1} is the complex conjugate of Z_{in1} , resulting in (13). By properly choosing the device parameters to satisfy (13), the input stage of the LNA exhibits a noise factor of F_{min} while maintaining a maximum power gain and a low input return loss at the operating frequency ω .

From (11), the noise factor decreases when g_m increases, this can be explained by the fact that ω_T increases as the g_m grows. It can be easily found that the larger bias resistor, the smaller noise factor will be. Fig. 3 (b) shows that the noise figure (NF) is smaller when R_b equals to 10 k Ω to compare with the case without R_b .

$$\frac{g_{m1}}{C_{gs1}} L_S = \frac{\sqrt{\frac{\alpha^2\delta}{5\gamma}(1 - |C|^2)}}{\omega_o C_{gs1} \left[\frac{\alpha^2\delta}{5\gamma}(1 - |C|^2) + \left(1 + \frac{\alpha^2\delta|C|^2}{5\gamma}\right)^2 \right]}. \quad (13)$$

In addition, as previously mentioned, the inter stage amplifier acts as a Three-stage amplifier. The NF of the third stage is influenced by both the MOSFETs (M_2 and M_4) and the inductor L_1 can be reduced by the gain of the

first stage. In addition, the NF originated from L_3 is reduced twice by the gains of the first and second stages and the NF originated from L_o is reduced thrice by the gains of the first, second and third stages. With this design technique, not only an ultra high gain can be obtained, a low NF can also be achieved simultaneously [8].

2.4 CMOS Implementation

By using 0.18 μm CMOS technology, the width of M_1 , M_2 and M_3 are determined as 160 μm , 200 μm and 120 μm respectively and M_4 is selected as 40 μm , smaller than M_2 to reduce parasitic capacitances. The inductors L_s and L_g are 204 pF and 0.3 nH, respectively. The inductors L_1 and L_3 are 2.1 nH and 0.43 nH respectively and the capacitor C_b is 10 pF. The output matching network inductor L_o of 1.35 nH and capacitor C_o is 0.15 pF. All inductors are realized with the on-chip spiral inductor structure.

3 Simulation results

The proposed LNA has been simulated by HSPICE RF using 0.18- μm CMOS process BSIM3 model parameters. The LNA operates with the 1.8 V power supply and consumes 16 mW power. Fig. 2 (a) presents the simulated input and output reflection coefficients. The NF and S_{21} parameters are depicted in Fig. 2 (b) and Fig. 2 (c), respectively.

At 5.7 GHz, this LNA has noise figure (NF) of 1.85 dB, voltage gain of 32.5 dB, with input return loss of -14 dB, output return loss of -17.5 dB, The isolation S_{12} is less than -56 dB over the bandwidth. To evaluate the performance of low noise figure LNAs, different figures of merit (FOMs) are commonly used in the literature. One figure of merit (FOM_1) of the LNA is the ratio of the gain in dB to the noise figure in dB. The LNA described in this letter has a value of 17.57 for this FOM_1 . Furthermore, it can be extended to include the supply voltage and operating frequency:

$$\text{FOM}_2 = \frac{\text{Freq}(\text{GHz}) \times \text{Gain}(\text{abs})}{\text{NF}(\text{abs}) \times V_{dd}(\text{v})}. \quad (14)$$

Table I. Performance summary and comparison to other CMOS LNA.

(a)

Ref.	This work	[2]	[3]	[4]	[5]	[9]	[10]
$F_0(\text{GHz})$	5.7	5.7	5.2	5.7	5.4	5.2	5.2
NF(dB)	1.85	3.5	2.45	3.7	3	2.5	3
$S_{21}(\text{dB})$	32.5	16.4	19.3	12.5	21	16	10
$S_{11}(\text{dB})$	-14	-11	N/A	-15	-10	-12	-30
$S_{22}(\text{dB})$	-17.5	-15	N/A	-9	N/A	-12	-15
$V_{dd}(\text{v})$	1.8	1	3.3	1.8	1.8	3	2
FOM_1	17.57	4.68	7.88	3.38	7	6.4	3.33
FoM_2	87.28	16.8	8.26	5.69	16.8	11.1	4.1

Fig. 2. Simulation results: (a) S_{11} , S_{22} parameters versus signal frequency, (b) Noise Figure versus signal frequency with and without R_b , (c) power gain versus signal frequency with proposed inter stage.

As indicated from Table I, our proposed LNA has the highest FOM_2 of 87.28. Simulation Results represent that the designed LNA has extremely high voltage gain, low noise figure, good input and output matching. The performance summary and comparison to other CMOS LNAs is listed in Table I.

4 Conclusion

In this paper, a 5.7 GHz low noise figure ultra high gain CMOS LNA with inter stage topology was presented where the common-source transistor inter-stage network is proposed. The new inter stage network improves, the noise and gain performance, providing dual functions of impedance match and DC current sharing. A bias resistor of large value is placed between source and the body node to prevent body effect and reduce noise. The implemented 0.18- μm CMOS LNA achieves -14 dB and -17.5 dB input and output return loss respectively. Compared with previously published current-reused LNA, the proposed technique improves the NF, gain and power dissipation with the number of 24.5%, 68.4% and 39.4% respectively.