A digital phase corrector with a duty cycle detector and transmitter for a Quad Data Rate I/O scheme

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Abstract: A digital phase corrector is proposed to reduce the time jitter noise in a high speed parallel chip-to-chip interface system with a quad data rate (QDR) input/output (I/O) scheme. The proposed digital phase corrector for the 4-phase clock utilizes only one duty cycle detector by using a digitally controlled phase correction method and multiplexing function of transmitter for a QDR I/O scheme. Also, it reduces the static phase error generated in the transmitter, because of the inclusion of a replica of the transmitter in the feedback loop. To verify the proposed digital phase correction scheme, a digital phase corrector for the QDR I/O scheme with a 1.25 GHz 4-phase clock was designed by using a 70 nm 3-metal CMOS process with a 1.35 V supply. The current consumption and phase correction range were 2.73 mA and $\pm 8\%$, respectively.

Keywords: phase corrector, transmitter, QDR I/O, duty cycle detector

Classification: Integrated circuits

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1 Introduction

As the chip-to-chip interface speed of a memory system and serial link system increases, the power consumption and area for the input/output (I/O) circuit design continuously increase. Thus, the multi-phase clock scheme utilizing a multi-phase clock generator, such as a phase locked loop (PLL) or delay locked loop (DLL), and multiplexers/de-multiplexers is used to reduce the power consumption of the clock signal in a high speed interface [1, 2]. Actually, the synchronous dynamic random access memory (SDRAM) reported in the literature [3] adopted a quad data rate (QDR) I/O scheme which used a multi-phase PLL for a 1.45 GHz 4-phase clock and 4-to-1 multiplexers/de-multiplexers for data and clock signals. However, the phase skew error among multi-phase clocks is generated due to the mismatch among delay cells for multi-phase clock generator and the mismatch between the pull up and pull down paths of the clock buffers. This phase skew error among multi-phase clocks causes the time jitter noise in the data and clock signals when a QDR I/O scheme is used. Thus, the implementation of a phase correction in the circuit of the high speed interface with multi-phase clocks is required to eliminate this error and thus enhance the performance of the high speed interface.

The ideal phases of four clocks ($CLKT[3:0]$) for a QDR I/O scheme are 0° , 90° , 180° , and 270° . In these cases, the phase error corrections between $CLKT[0]$ and $CLKT[2]$ and between $CLKT[1]$ and $CLKT[3]$ have the differential relations and thus are achieved by the duty cycle correction. Then, the phase error correction between $ICLK$ ($CLKT[0]$, $CLKT[2]$) and $QCLK$ ($CLKT[1]$, $CLKT[3]$) is achieved by the quadruple phase correction. Hence two duty cycle correction processes and one quadruple phase correction process are required for the phase-error correction of a 4-phase clock. The conventional phase correction scheme requires a separated phase error detector for each phase correction process, because these three phase correction processes are achieved simultaneously. It increases the power consumption, area, and the sensitivity to many noise sources because duty cycle detectors and quadruple phase detectors are implemented by analog circuits.

In this paper, a digital phase corrector for a QDR I/O scheme is proposed. It uses only one duty cycle detector, which uses a digitally controlled phase correction method and multiplexing function of transmitter for the QDR I/O scheme. It also results in the minimization of the usage of analog circuit and the subsequent reduction of area, power consumption, and noise sensitivity. This paper is organized as follows: In Section 2, the proposed digital phase corrector is discussed. Section 3 shows the design and simulation results of the test chip, and finally in Section 4, the conclusion of this paper is presented.

2 Proposed digital phase corrector

The proposed digital phase corrector uses only one duty cycle detector instead of the three phase error detectors for the three phase correction processes for a 4-phase clock. To detect all phase errors by using only one duty cycle detector, the digital phase correction method and a replica of the transmitter

for a QDR I/O scheme are used in this work. Fig. 1 (a) is the block diagram of the proposed digital phase corrector for a QDR I/O scheme with a 1.25 GHz 4-phase clock, which supports the interface speed of 5.0 Gbps. The proposed digital phase corrector is divided into two parts, the phase error detection and the phase error correction parts. The phase error detection part is composed

Fig. 1. (a) Block diagram of digital phase corrector (b) Three phase correction processes according to input data pattern of TX replica (c) Current integrator of duty cycle detector (d) Timing diagram of current integrator

of a *TX replica*, a *Duty cycle detector*, and a *Register*. Also, the phase error correction part is composed of two duty cycle correctors (DCC - *DCCI*, *DCCQ*), two quadruple phase correctors (QPC - *QPCI*, *QPCQ*), and a *Clock Driver* which is composed of a CML-to-CMOS converter and a CMOS buffer.

The proposed digital phase correction is achieved by three sequential correction processes instead of the conventional phase correction achieved by three parallel processes. Each phase correction process is controlled by the pre-determined *REP_DAT[3:0]* signal supplied to *TX replica*. In each phase correction process, the phase error information is detected by the *Duty cycle detector*, which measures the duty cycle of the output signal of the *TX replica*, *OTX_REP*. Fig. 1 (b) shows three phase correction processes according to the input data pattern of the *TX replica*. In the first phase correction process, the data pattern of “1100” for *REP_DAT[3:0]* signal is used to detect the phase error between *CLKT[0]* and *CLKT[2]*. Then the differential phase corrector for the *ICLK* (*CLKT[0]* and *CLKT[2]*), *DCCI*, is controlled so that the *OTX_REP* differential signal has the duty cycle of 50%. In the second phase correction process, the data pattern of “0110” for *REP_DAT[3:0]* signal is used to detect the phase error between *CLKT[1]* and *CLKT[3]*. In this case, *DCCQ* is controlled by the digital control code supplied from the *Register*. In the last phase correction process, the quadruple phase error between *CLKT[0]* and *CLKT[1]* is detected by using the data pattern of “1010” for the *REP_DAT[3:0]* signal. *QPCI* and *QPCQ* are simultaneously controlled by the complementary digital code for the quadruple phase relationship between the *ICLK* and *QCLK*. In this process, the duty cycle of the *ICLK* and *QCLK* should be maintained, and the delay difference between the *ICLK* and *QCLK* should be only controlled. To meet these requirements, the phase correctors for the duty cycle correction, *DCCI* and *DCCQ*, are composed of the 4-input differential amplifier [4]. The control signals for the 2-input are controlled by the digital codes, *DCCI[4:0]* and *DCCQ[4:0]*. Also, the phase correctors for the quadruple phase relationship, *QPCI* and *QPCQ*, are composed of the 2-input differential amplifier. The control codes for them, *QPC[4:0]* and */QPC[4:0]*, are supplied to control the tail current of the 2-input differential amplifier.

In the proposed phase correction scheme, the phase correction information of each process should be stored as the digital code in the register to sequentially process the three phase correction. For the digitally controlled phase correction process, the duty cycle detector is composed of a current integrator shown in Fig. 1 (c), a voltage comparator, and a 5-bit counter [5]. The operating clock for the current integrator, *CLKI*, is the clock divided by two from one clock among 4-phase clock (*CLK[3:0]*) and the timing diagram of the current integrator is shown in Fig. 1 (d). When the outputs of current integration (*VOP*, *VOM*) are equal, *OTX_REP* signal has the duty cycle of 50%. The duty cycle detector generates 5-bit digital code that corresponds to the difference of the duty cycle of *OTX_REP* signal from 50%.

The phase error detector is generally composed of the analog block which is sensitive from the process, voltage, and temperature (PVT) variation. In

the proposed digital phase corrector, one current integrator and one voltage comparator are used. Thus the proposed digital process scheme makes the calibration scheme simpler and reduces the area of the analog block. Also, the replica of the transmitter can be removed by controlling the normal transmitter in the phase correction mode. In this case, the output of the normal transmitter should be connected to the duty cycle detector and the input of the normal transmitter should be controlled by the *Data Logic* block for three phase correction processes, as shown in Fig. 1 (b). The proposed digital phase corrector reduces the static phase error, which is generated in the transmitter, because the feedback loop of the proposed digital phase corrector includes the replica of the transmitter. Thus the proposed digital phase corrector removes the time jitter noise in the data and clock signals of QDR I/O schemes due to a multi-phase error.

3 Chip Design and Simulation results

The proposed digital phase corrector was designed by using a 70 nm 3-metal CMOS process with a 1.35 V supply. The QDR I/O scheme using a 1.25 GHz 4-phase clock supports the interface speed of 5.0 Gbps. Fig. 2 shows the designed layout, which additionally increased because of the global clock buffer. For the digitally controlled three phase correction processes, three register blocks were used and a counter block was shared. Table I summarizes the

Fig. 2. Layout of digital phase corrector

Table I. Comparison of phase corrector area

Layout Area	Conventional Architecture [μm^2]	Proposed Architecture [μm^2]
DCCI, DCCQ (with global clock buffer)	2,300 (9,200)	
QPCI, QPCQ, Clock Driver	2,480	
Phase Error Detector	2,230×3	2,470×1
TX Replica	0	700 (TX×1/10)
Counter & Register	3,600	
Toal Area	15,070	11,550 (w/ TX Replica) 10,850 (w/o TX Replica)

layout based area excepting the global clock buffer. The proposed digital phase corrector reduced the area of about 23% compared to the conventional architecture when the replica of transmitter has one tenth the size of the normal transmitter. Also, the area reduction achieved by the proposed scheme increased to 28% when the replica of transmitter block was replaced with the normal transmitter.

The current consumption excepting the global clock buffer was 2.73 mA at the operation speed of 5.0 Gbps, which is a 36% reduction when compared to the conventional architecture. The phase correction range and control resolution of the DCC and QPC were $\pm 8\%$ and 4 ps, respectively. Fig. 3 show the output waves in some cases when the duty cycle error and quadruple phase error of the 4-phase clock with a 1.25 GHz are 3%, respectively. The worst data eye is generated when the duty cycle error and quadruple phase error exist together, as shown in Fig. 3 (a). Fig. 3 (b) shows the output wave corrected by the proposed digital phase corrector.

Fig. 3. Output wave according to phase skew (a) with duty cycle error and quadruple phase error (b) after 4-phase skew correction

4 Conclusion

A digital phase corrector was proposed for a high speed parallel interface with a QDR I/O scheme. The proposed digital phase corrector for the 4-phase clock utilized only one duty cycle detector by using a digitally controlled phase correction method and multiplexing function of transmitter for a QDR I/O scheme. Thus the proposed digital phase correction scheme reduced the

area, current consumption, and design complexity by minimizing the use of analog blocks. Also, it reduced the static phase error generated in the normal transmitter because of the inclusion of the replica of the transmitter in the feedback loop of the proposed phase corrector. To verify the proposed digital phase correction scheme, the digital phase corrector for the QDR I/O scheme with a 1.25 GHz 4-phase clock was designed by using a 70 nm 3-metal CMOS process with a 1.35 V supply. The current consumption and phase correction range were 2.73 mA and $\pm 8\%$, respectively.

Acknowledgments

This paper was supported by Research Fund, Kumoh National Institute of Technology.