Transformer feedback millimeter-wave VCO with capacitance cancellation technique in 0.18- μm CMOS

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Abstract: This paper describes a design procedure for mm-wave voltage controlled oscillator (VCO), based on large signal behavior of oscillator transconductance. Then, a new structure of LC-VCO is presented, which utilizes a transformer feedback to enhance the transconductance of the core transistors and to cancel the undesired parasitic effects. Using a 0.18- μm RF CMOS technology, the advantage of this VCO is examined by large signal analysis and simulation. The results illustrate improvement of 5 dB in phase-noise and 70% in tuning-range, compared to enhanced active gain conventional transformer feedback VCO. Finally, a compact layout for transformer design is proposed.

Keywords: millimeter-wave, VCO, transformer feedback

Classification: Integrated circuits

References

- [1] M. Fujishima, “Recent trends and future prospective on millimeter-wave CMOS circuits,” *IEICE Electron. Express*, vol. 6, no. 11, pp. 721–735, June 2009.
- [2] H.-C. Chiu and C.-P. Kao, “A Wide Tuning Range 69 GHz Push-Push VCO Using 0.18 μm CMOS Technology,” *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 2, pp. 97–99, Feb. 2010.
- [3] H.-H. Hsieh and L.-H. Lu, “A V-Band CMOS VCO With an Admittance-Transforming Cross-Coupled Pair,” *IEEE J. Solid-State Circuits*, vol. 44, no. 6, pp. 1689–1696, June 2009.
- [4] Y. Tajima, B. Wrona, and K. Mishima, “GaAs FET large-signal model and its application to circuit designs,” *IEEE Trans. Electron Devices*, vol. 28, pp. 171–175, 1981.
- [5] Y. Tsividis, *Operation and Modeling of The MOS Transistor*, 2nd edition, Oxford University Press, June 2003.
- [6] Dickson, et al., “The Invariance of Characteristic Current Densities in Nanoscale MOSFETs and Its Impact on Algorithmic Design Methodologies and Design Porting of Si(Ge) (Bi)CMOS High-Speed Building Blocks,” *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1830–1845,

- Aug. 2006.
- [7] Y. Chen, K. Mouthaan, and F. Lin, “Design of X-Band and Ka-Band Colpitts Oscillators Using a Parasitic Cancellation Technique,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 1817–1828, Aug. 2010.
 - [8] B. Razavi, “A Millimeter-Wave Circuit Technique,” *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 2090–2098, Sept. 2008.
 - [9] Dickson, et al., “30–100-GHz inductors and transformers for millimeter-wave (Bi)CMOS integrated circuits,” *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 1, pp. 123–133, Jan. 2005.
 - [10] C. P. Yue and S. S. Wong, “Physical modeling of spiral inductors on silicon,” *IEEE Trans. Electron Devices*, vol. 47, no. 3, pp. 560–568, March 2000.
 - [11] P. Andreani and S. Mattisson, “On the use of MOS varactors in RF VCOs,” *IEEE J. Solid-State Circuits*, vol. 35, no. 6, pp. 905–910, June 2000.

1 Introduction

The availability of bandwidth that enables multi-Gb/s wireless communication in the 60 GHz spectrum has motivated RF Engineers to design various CMOS transceivers in this millimeter-wave band [1]. One of the challenging problems in these transceivers is designing low-power and area efficient VCO with low phase noise and large tuning range. However, the requirements for this performance are affected by passive element losses and the gain limitation of active devices in the 60 GHz band. Using large sized transistors to achieve higher gain is not often a proper alternative. Also, utilizing large sized MOS varactors for tuning range improvement leads to phase noise degradation due to their low quality factor. Therefore, a severe tradeoff exists between oscillation frequency, phase noise, and tuning range.

Recently, various designs have been proposed to increase the gain of the core transistors in millimeter-wave VCOs by overcoming the above mentioned tradeoff [2, 3]. A push-push oscillator is presented in [2], in which the oscillation frequency is as twice as the resonance frequency of the LC-tank. This gives the possibility of the MOS transistors to operate at lower frequencies while having higher gains, and also the increase in quality factor of the varactors. Unfortunately, this topology suffers from single-ended or imperfect differential output with abated output power. Utilizing a transmission line as an admittance transformer [3] may provide higher negative conductance with small sized transistors. However, distributed circuits are often area inefficient and power hungry.

In this paper, a new transformer feedback differential LC-VCO is proposed, in which the inductance of the transformer is utilized to partially cancel the undesired parasitic capacitances and to enhance the negative transconductance of the active devices. Also, a compact layout for transformer design is proposed.

2 Design procedure and oscillator topology:

The main target in designing a millimeter-wave VCO is devoted to relax the start-up and to improve the phase noise. To achieve this, we utilize a design procedure which maximizes the negative transconductance for a generic millimeter-wave oscillator, depicted by the half circuit model in Fig. 1 a. In this circuit, the transistors widths and the feedback factor must provide adequate gain within the entire band. However, a large bias current needs wide transistor to preserve the current density associated with maximum frequency f_{max} . On the other hand, large parasitics in wide transistors may severely impair both the tuning range and the phase noise performance at mm-wave band.

Fig. 1. a) Half circuit of the generic VCO b) Conventional transformer feedback VCO.

According to the half-circuit model of Fig. 1 a, transconductance (G_m) and capacitance (C) seen from the drain of M_1 can be derived as follows.

$$G_m = g_{ds}(v) - g_m(v) \times k \quad (1)$$

$$C = C_{ds} + C_{gd} \times (k + 1) \quad (2)$$

where C_{ds} , C_{gd} , C_{gs} (which are directly related to the width of the transistor) are drain-source capacitance, gate-drain capacitance, gate-source capacitance, respectively. Also, k denotes the feedback gain, $g_m(v)$ represents the large signal transconductance of transistor, and $g_{ds}(v)$ is large signal output conductance. To realize the feedback gain, we utilize two highly coupled inductors, $L1$ and $L2$ (Fig. 1 b). Thus the feedback gain factor can be calculated as $k = \sqrt{L2/L1}$. For calculating G_m , we can write the drain current $i_d = f(V_{gs}, V_{ds})$ with defining a describing function or method used in [4] as:

$$i_d(\omega t) = I_0 + g_m(V_{gs}, V_{ds})v_{gs} \times \sin(\omega t + \varphi) + g_{ds}(V_{gs}, V_{ds})v_{ds} \times \sin(\omega t) \quad (3)$$

where I_0 , V_{gs} , and V_{ds} are DC current and sum of DC and AC voltage of gate-source and drain source, respectively. φ is phase difference between gate and drain, which depends on transistor capacitors and conductance. Multiplying

two sides of Eq. (3) by $\cos(\omega t)$ and $\cos(\omega t + \varphi)$ and integrating in one period, g_m and g_{ds} are obtained by:

$$\begin{aligned} g_m &= \frac{1}{\pi \times v_{gs} \times \sin(\varphi)} \int_0^{2\pi} i_d(\omega t) \cos(\omega t) d(\omega t) \\ g_{ds} &= \frac{-1}{\pi \times v_{ds} \times \sin(\varphi)} \int_0^{2\pi} i_d(\omega t) \cos(\omega t + \varphi) d(\omega t) \end{aligned} \quad (4)$$

$i_d(\omega t)$ can be modeled by [5]:

$$i_d(\omega t) = \frac{K_0}{1 + \theta(V_{gs} - V_t)} \frac{W}{L} (V_{gs} - V_t)^2 (1 + \lambda \times V_{ds}) \quad (5)$$

where, V_t is threshold voltage, K_0 is a technology constant, λ is channel length modulation parameter, and θ is used to model mobility degradation due to vertical field. With some iterations between Eq. (4) and φ , minimum of G_m is obtained for $k = 2$ and $W = 17 \mu\text{m}$ in 60 GHz, 2.2 mA DC drain current, and 0.7 V of output amplitude. The current density for minimizing G_m is coincided with current density achieved in [6] for maximizing f_{max} of transistor. In order to appraisal the behavior of the negative- G_m block under large signal and high frequency operation, large signal simulations are exploited. Fig. 2a shows the equivalent G_m of the half circuit. As illustrated in Fig. 2a, G_m reaches its minimum value for $k = 2.5$ and transistor width

Fig. 2. Half circuit large signal simulation results of (a) generic oscillator G_m (b) generic oscillator capacitance (c) G_m of oscillator with cancellation technique (d) capacitance of oscillator with cancellation technique.

$W = 16 \mu\text{m}$ which are concurred with analytical expression. Fig. 2 b depicts parasitic capacitance of the half circuit. As shown in this figure, the parasitic capacitance is monotonically increased with W and k . This leads to deterioration of tuning range and phase noise performance of the VCO. Employing an inductor between the gate and the drain of each MOS transistor in series with a dc decoupling capacitance (C_d) can partially cancel the parasitic capacitance [7]. The effective transconductance and the total capacitance can be defined as:

$$G_m \approx g_{ds}(v) - g_m(v) \times k + \frac{(k+1)}{L_C \omega Q_C} \quad (6)$$

$$C \approx C_{ds} + C_{gd} \times (k+1) - \frac{(k+1)}{L_C \times \omega^2} \quad (7)$$

where L_C and Q_C are the canceling inductance and its quality factor, respectively. Taking the advantages of Eq. (6) and (7) and performing the large signal simulations, it can be shown that by using $L_C = 700 \text{ pH}$ with quality factor of 15, large amount of parasitic capacitances in negative G_m stage can be canceled without significant impact on G_m (Fig. 2 c, d).

To avoid the designing of additional inductor, one can use the single side of transformer as canceling inductor. Now by merging L_C with L_2 , we realize the transformer feedback oscillator in Fig. 3 a, which can provide parasitic cancelation without adding any extra inductor. Since L_2 in this oscillator may not have the exact value for full parasitic cancellation, the parasitics are partially neutralized. Nevertheless, this partial cancellation will extent the tuning range, and gives the possibility of using a larger resonator inductance. Thus, the phase noise is reduced by increasing the oscillation amplitude. Additionally, the small impedance from the gate-to-drain of the core transistors at low frequencies prevents the phase difference resulted from gate flicker noise [8]. As explained in the next section, this transformer can be implemented with the same area required for one inductor.

The conventional transformer feedback VCO (Fig. 1 b) and the proposed VCO (Fig. 3) are simulated for identical current sources, core transistors, varactors and feedback gain (we choose $k = 2$ and $W = 16$). The oscillation frequency is $\omega_0 = 1/\sqrt{L_1 \times (C_{ds} + C_{gs} + (C_{gd} + C_{gs}) \times k^2 + 2 \times C_{gd} \times k)}$ for the Conventional VCO (Fig. 1 b) and $\omega_0 = 1/\sqrt{L_1 \times (C_{ds} + C_{gs} + (C_{gd} + C_{gs})k^2 - 2 \times C_{gs} \times k)}$ for the proposed (Fig. 3 a) VCO. Although the oscillation bands of these two VCOs must be the same, the resonator inductance of the proposed VCO (L_1) is twice of the first one. Oscillators' phase noise and tuning range are depicted in Fig. 3 b. This figure illustrates that the tuning range (TR) and phase noise (PN) of the new VCO are improved by about 70% and 5 dB at 1 MHz, respectively, in comparison with the conventional transformer feedback VCO. Also, phase noise simulations suggest 3.5 dB improvement at 10 MHz offset for new VCO. These advantages stem from the canceling technique of the parasitics. Simulations show that the proposed circuit also displays good performance at other bias conditions.

Fig. 3. a) The transformer feedback oscillator with parasitic cancelation technique b) Phase Noise (PN) and Tuning Range (TR) of VCO with Canceling technique (VC) (solid line), and the conventional Transformer feedback VCO (TV) (dashed line). c) Proposed transformer design and its formation manner from L1–L4 (heights are not scaled for better illustration).

3 Transformer design

Substrate-induced loss is the dominant loss in spiral inductors at millimeter-wave frequencies [9]. Thus, the transformer should be designed as compact as possible to minimize the loss mechanism.

Coupling factor can inversely be related to geometric mean distance (GMD) between the pair inductors defined by [10]:

$$\ln GMD = \ln d - \frac{w^2}{12d^2} - \frac{w^4}{60d^4} - \frac{w^6}{168d^6} - \dots \quad (8)$$

where w and d are metal width and pitch, respectively. A transformer with high coupling factor can be realized using stacked inductors, since its GMD between the pair inductors is lower than tapered transformer. Calculating coupling factor through electromagnetic formulation illustrates that the coupling factor of stacked transformer is as twice as tapered transformer. Stacked

implementation requires small area, alleviates substrate-induced losses, and improves the quality factor of the inductors. Since varactors dominate the quality factor of the resonator at millimeter-wave frequencies, a resonator inductor with a quality factor larger than 10 slightly affect the overall resonator quality factor. Therefore, we decide to implement the resonator inductors ($L1$, $L3$) and feedback inductors ($L2$, $L4$) symmetrically with metal 5 and metal 6, respectively. We designed resonator inductors ($L1$, $L3$) differentially (Fig. 3 c). To realize the above mentioned feedback factor (k), small resonator inductances ($L1$, $L3$) and large feedback inductances ($L2$, $L4$) are used. For realization of dissimilar inductances values, the metal width of ($L1$, $L3$) is chosen wider than ($L2$, $L4$). The inductor with larger metal width may generate less magnetic flux; therefore, it has lower inductance. However, its metal resistance decreases and the quality factor of transformer inductor is enhanced. The metal width of $L1$ and $L2$ are $12\ \mu\text{m}$ and $6\ \mu\text{m}$, respectively. Although ($L2$, $L4$) have narrower widths with a higher metal loss, they show lower substrate loss which gives the possibility of increasing their quality factors. As a result, the third term in Eq. (6) can be vanished. This transformer is simulated with Agilent Momentum, $L1$, $L2$, and coupling factors are equal to 75 pH, 200 pH, and 0.75, respectively. The value of Q_1 and Q_2 is slightly larger than 15 and 22, respectively, and the area of this transformer is only $100\ \mu\text{m} \times 100\ \mu\text{m}$.

4 Simulation results

EM simulations are used to extract the transformer S parameters. In this transformer, $L2$ has superior Q compared to conventional transformer, used in the previous simulations. After EM analysis, some extra parasitic capacitance is also added, and practical k and coupling factor are found. Therefore, the transformer feedback VCO with cancelation technique is redesigned and simulated using a $0.18\text{-}\mu\text{m}$ RF CMOS process with the EM extracted parameters of transformer. Since at mm-wave frequencies the hole generation problem, observed in few gigahertz frequencies, is almost vanished [11], we use a simple minimum length PMOS transistor instead of an AMOS varactor to tune the VCO. To drive a $50\ \Omega$ load, a two-stage common-source output buffer [3] is employed.

The supply voltage is equal to 1.8 V, and the core power consumption of the VCO is 11.5 mW. The simulated tuning range is equal to 3.8 GHz (57.9–61.7 GHz) and the phase noise is from $-93\ \text{dBc/Hz}$ to $-85\ \text{dBc/Hz}$ at 1 MHz offset within the entire band. The output delivered power of this oscillator on a $50\ \Omega$ load is about $-12\ \text{dBm}$. The common figure of merit for oscillator [7] of the simulated circuit is nearly $-175\ \text{dBc/Hz}$.

5 Conclusion

In this paper the parasitic cancelation technique in millimeter-wave transformer feedback VCO has been proposed, which simultaneously improves the tuning range and phase noise. It uses a transformer feedback which partially

cancels out the parasitic capacitance and enhances the negative- G_m of the active core devices. Simulation results of the proposed VCO using a 0.18- μm RF CMOS process along with electromagnetic analysis of the transformer illustrate 4 GHz tuning range around 60 GHz, -90 dBc/Hz phase-noise at 1 MHz offset, and a DC power consumption of nearly 11.5 mW.

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