A novel CMOS high accuracy fast speed OTA for switched-capacitor filters

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Abstract: A novel high accuracy fast speed operational transconductance amplifier (OTA) for switched-capacitor filters in 0.35 μm CMOS technology is presented in this paper. The proposed OTA employs non-linear current mirror and cross-pair structure to enhance the DC, AC and transient performance. Both simulation and experimental results are presented to show the performance boosting of the proposed OTA. Under the condition of 33 μA quiescent current and a 30 pF load capacitance, the experimental results of the DC gain, Gain Bandwidth, positive and negative slew rate have achieved as high as 62.5 dB, 4.9 MHz, 6.3 V/μs and 8 V/μs, respectively. Both GBW and SR are boosted more than one order compared to the conventional OTA.

Keywords: operational transconductance amplifier, nonlinear current mirror, cross-pair

Classification: Integrated circuits

References


1 Introduction

Operational transconductance amplifiers (OTAs) are widely employed to drive large capacitive loads in many switched-capacitor filter applications where both accuracy and speed are needed. For accuracy, high voltage gain is required, and for speed, wide band and high slew rate are needed. It is impossible for conventional OTA to obtain all these requirements simultaneously, especially under the constraints of small static power consumption. Since the slew rate of conventional OTA as given by \(SR = \frac{I_B}{C_L}\) is limited by tail current \(I_B\) for the load capacitor \(C_L\) charging. An effective way to improve SR is using adaptive tail current [1, 2] or using SRE (Slew Rate Enhancement) technique [3], but neither of them has the improvement to the AC performance. In this paper, a single-stage high accuracy, fast speed OTA is proposed by simply integrating nonlinear current mirror and cross-pair effects together, which is particularly suitable for CMOS filter circuits.

2 Proposed OTA topology

Figure 1 shows the proposed OTA structure. It can be obtained from conventional OTA by adding a couple of cross-pair [4, 5] (M7, M8) and replacing the linear current mirror with the adaptive nonlinear current mirror [6] (M3/M4, M5/M6, M9/M10). If the W/L ratio of M9/M10 is scaled as unit, the scaled W/L ratios of M5a/M6a, M5b/M6b and M7/M8 are \(N_S\), K and K, respectively. \(V_A\) and \(V_B\) are the voltage at node A and B.

Since the positive feedback cross-pair used, in small signal approxima-
tion, the effective W/L ratio of load diode transistors are given by $N_{eff} = N_S + (K+K)$, where the selection of “±” is signal or operation mode related. Under the DC condition, because of the symmetry of the OTA with $V_A = V_B$, “+” is selected to give $N_{DC} = N_S + 2K$, therefore, the static output current is reduced by a larger $N_{DC}$. When entering the AC situation with $\Delta V_A = -\Delta V_B$, “−” is selected to give $N_{AC} = N_S$, which leads to a large AC output current by a smaller $N_{AC}$, as respect to the conventional OTA with $\alpha_{AC} = 1$, a multiplied factor of $\alpha_{AC} = N_{DC}/N_{AC}$ is obtained. When the input signal exceeds the maximum dynamic range, one transistor in the cross-pair cuts off and the other one enters into triode resistance region, and neither of them has current flowing, so the cross-pair becomes invalid and the effective W/L ratio of load diode transistors shift from $N_{DC}$ to $N_{DY} = N_S + K$, then a factor as $\alpha_{DY} = N_{DC}/N_{DY}$ is introduced.

Except the cross-pair structure, the nonlinear current transportation can also improve the output current significantly. When transistors $M5a/M6a$, $M5b/M6b$, $M7/M8$ are biased in triode resistance region by decreasing voltage $V_{bn}$, the original linear current mirror turns into nonlinear one. Supposing that $\Delta M_{5a}$ and $V_{DS_{5a}}$ are the overdrive voltage and the drain voltage of the transistor $M5a$, respectively and $\Delta M_{B1}$ is the overdrive voltage of transistor $M_{B1}$. State factors of current mirror are defined as $\alpha = \Delta M_{5a}/\Delta M_{B1}$ and $\eta = V_{DS_{5a}}/\Delta M_{B1}$, respectively, and the critical condition for the current mirror shifting from linear to nonlinear is given by $\alpha \geq \eta$.

According to the saturation current equation of $M9$ ($M10$), we have

$$I_9 = \frac{1}{2} k_9 (V_{GS9} - V_{TN9})^2 = \frac{I_3}{N_{DC}} P_{DC} \left( \frac{\alpha}{1 - \zeta \eta} \right)^2$$

$$= \frac{I_3}{N_{DC}} \beta_{DC}$$

(1)

where $P_{DC} = ((W/L)_{M5a} + (W/L)_{M5b} + (W/L)_{M7} + (W/L)_{M8})/((W/L)_{M3})$ and $\gamma$ is the substrate biasing coefficient and $\zeta = 1 + \gamma$. The total static current of the new OTA can be expressed as $I_Q = I_B(1 + \beta_{DC}/N_{DC})$. Larger $\alpha$ or smaller $\eta$ leads to larger $\beta_{DC}$, and the static current increases more due to the deeper nonlinear effect. Taking the derivation of equation (1), the current transmission coefficient of the nonlinear current mirror shifting from DC to AC is given by

$$\frac{\partial I_9}{\partial I_3} = \frac{1}{N_{AC}} \left( \beta_{DC} + I_3 \frac{\partial \beta_{DC}}{\partial \alpha} \frac{\partial \alpha}{\partial I_3} \right) = \frac{\beta_{AC}}{N_{AC}}$$

(2)

where $\beta_{AC}$ represents the increase of AC current due to the nonlinear current mirror effect which can be expressed as $\beta_{AC} = (1 + m) \beta_{DC}$ and the additional positive factor $m = I_3(\partial \beta_{DC}/\partial I_3)$ which makes $\beta_{AC} > \beta_{DC}$. $m$ is improved with $\alpha$ increasing. The total transconductance of the OTA can be written as

$$G_m = g_{m1,2} \frac{\partial I_9}{\partial I_3} = g_{m1,2} \frac{\beta_{AC}}{N_{AC}} = g_{m1,2} \frac{N_{DC}}{N_{DC}} \frac{N_{AC}}{N_{AC}} \beta_{AC} = (\alpha_{AC} \beta_{AC}) G_{m_{ref}}$$

(3)

where $G_{m_{ref}} = g_{m1,2}/N_{DC}$; $g_{m1,2}$ and $G_{m_{ref}}$ are the transconductance of the differential pair and the referenced conventional OTA, respectively. Since the
unity gain bandwidth for single stage OTA can be written as \( \text{GBW} = \frac{G_m}{C_L} \), the boosting factor of GBW as respect to \( \frac{G_{m,ref}}{C_L} \) is also \( \alpha_{AC}\beta_{AC} \), which is limited by the second pole at node A (B). Similarly, we can obtain the DC gain and SR of the new OTA as

\[
A_V = \frac{G_m}{\lambda I_O} = \left( \frac{\alpha_{AC}\beta_{AC}}{N_{DC}\beta_{DC}} \right) A_{V,ref} \tag{4}
\]

\[
SR = \frac{I_O}{C_L} = (\alpha_{DY}\beta_{DY}) SR_{ref} \tag{5}
\]

In equation (4), \( A_V = \frac{G_{m,ref}}{(\lambda I_O)_{ref}} \) is the DC gain of the referenced conventional OTA and \( \lambda = \lambda_N + \lambda_P \), where \( \lambda_N \) and \( \lambda_P \) are the channel-length modulation coefficients of NMOS and PMOS. Considering the direct influence of static output current, the DC gain is also modulated by \( N_{DC} / \beta_{DC} \).

Supposing the settling time constant for unit negative feedback OTA is \( \tau = 1/(2\pi \text{GBW}) \), and \( V_S \) is the applied input step voltage during transient response, and \( V_{S,cr} = \tau \times \text{SR} \) is defined as the critical voltage swing. The settling time is unlimited by SR under the small signal condition of \( V_S \leq V_{S,cr} \), which can be written as

\[
t_{\text{settling}} = -\tau \ln(\varepsilon_d) = -\frac{V_{S,cr}}{SR} \ln(\varepsilon_d) \tag{7}
\]

where \( \varepsilon_d \) is the dynamical error for output voltage. Under the system stable limitation, large GBW or small \( \tau \) results in a fast small signal settling procedure in this situation. When entering into the large signal condition of \( V_S > V_{S,cr} \), the settling time is related to both SR and GBW, which can be given by

\[
t_{\text{settling}} = \frac{V_S}{SR} + \frac{V_{S,cr}}{SR} \left[ \ln \left( \frac{V_{S,cr}}{\varepsilon_d V_S} \right) - 1 \right] = \frac{V_S}{SR} + \tau \left[ \ln \left( \frac{\tau SR}{\varepsilon_d V_S} \right) - 1 \right] \tag{8}
\]

Clearly, the settling time also decreases with larger GBW as mentioned above, however, the first and second term in above equation varies contrarily with SR increasing, which results in a complicated settling characteristic. If SR increases to make \( V_S = V_{S,cr} \), the equation (8) is simplified to equation (7). Since a high SR generates a larger \( V_{S,cr} \), the close loop of OTA remains in small signal mode even with a relative large \( V_S \) (\( V_S < V_{S,cr} \)), finally the minimal settling time can be obtained by a maximal GBW.
In practical, the boosting factors as given in equation (3), (4) and (5) are limited due to the stability and the mismatch problems. Here, $\alpha_{AC}$, $\alpha_{DY}$ are device dimensions related and $\beta_{AC}$, $\beta_{DY}$ are circuit status related. In order to obtain a larger $\alpha_{AC}$ or $\alpha_{DY}$, a larger $K$ is needed, however, parasitic capacitance at node A (B) is increased, and hence a lower second pole. Besides, it is more difficult for devices matching in the nonlinear current mirror with $K$ increasing. On the other hand, if a larger $\beta_{AC}$ or $\beta_{DY}$ is required, a higher impedance at node A (B) will be formed by a higher $g_{d5}$ ($g_{d6}$), where $g_{d5}$ ($g_{d6}$) is the drain admittance of M5 (M6), and the second pole at node A (B) is decreased which limits the GBW of OTA. Therefore, a well designed OTA is a result of trade-off among the performance, the stability, the process robustness and the power consuming.

### 3 Simulation and experimental results

The proposed OTA was implemented in CSMC 0.35$\mu$m CMOS technology ($V_{TN}=0.7$ V, $V_{TP}=-0.95$ V). The supply voltage, load capacitor and the substrate biasing coefficient $\gamma$ are 5 V, 30 pF and 0.45, respectively. For the circuit we set $N_{DC}=1, P_{DC}=1, P_{DY}=7/12, \alpha=0.58, \eta=0.40, \alpha_{AC}=6,$

![Fig. 2. The experimental results of chip: (a) the actual GBW tested by spectrum analyzer, (b) the experimental waveforms of SR](image-url)

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**Fig. 2.** The experimental results of chip: (a) the actual GBW tested by spectrum analyzer, (b) the experimental waveforms of SR
\(\alpha_{DY}=12/7, \beta_{DC}=1.9\) and \(\beta_{AC}=2.9\) in static condition and \(\beta_{DY}=16\) in dynamical condition by suitable nonlinear control. Figure 2(a) and (b) show the actual GBW tested by the spectrum analyzer and the experimental waveforms of SR, respectively. In above situation, the calculated \(\tau=32\) ns, \(V_{S,cr}=0.26\) V, and the actual voltage swing \(V_S=0.6\) V (from 0.9 V to 1.5 V), the settling time calculated by equation (8) due to \(V_S>V_{S,cr}\) is 0.24 \(\mu s\), well fitted with the simulation and experimental results.

A referenced conventional OTA designed with the same W/L ratio of transistors, \(N_{DC}\) and the tail current is used for comparison with the proposed OTA. The circuit’s figure of merit in AC and transient operation mode are defined as

\[
FOM_{AC} = \frac{GBW(MHz)C_L(pF)}{I_{TOT}(\mu A)}
\]

\[
FOM_{DY} = \frac{SR(V/\mu s)C_L(pF)}{I_{TOT}(\mu A)}
\]

As shown in table I, all of the performance of the proposed OTA are boosted more than one order at the cost of 50% static current increased, as compared to the referenced OTA.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Conventional OTA Simulation results</th>
<th>Proposed OTA Simulation results</th>
<th>Proposed OTA Experimental results</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC gain</td>
<td>41.5 dB</td>
<td>63.8 dB</td>
<td>62.5 dB</td>
</tr>
<tr>
<td>GBW</td>
<td>305.8 kHz</td>
<td>5.6 MHz</td>
<td>4.9 MHz</td>
</tr>
<tr>
<td>Positive SR</td>
<td>0.4 V/\mu s</td>
<td>7.5 V/\mu s</td>
<td>6.3 V/\mu s</td>
</tr>
<tr>
<td>Negative SR</td>
<td>0.4 V/\mu s</td>
<td>10 V/\mu s</td>
<td>8 V/\mu s</td>
</tr>
<tr>
<td>0.1% settling time</td>
<td>4.84 (\mu s)</td>
<td>0.23 (\mu s)</td>
<td>0.25 (\mu s)</td>
</tr>
<tr>
<td>Quiescent current</td>
<td>23 (\mu A)</td>
<td>32 (\mu A)</td>
<td>33 (\mu A)</td>
</tr>
<tr>
<td>(FOM_{AC})</td>
<td>0.40V</td>
<td>5.25V</td>
<td>4.45V</td>
</tr>
<tr>
<td>(FOM_{DY})</td>
<td>0.52</td>
<td>9.38</td>
<td>7.5</td>
</tr>
</tbody>
</table>

4 Conclusion

In this paper a novel high accuracy fast speed OTA was proposed and verified in CSMC 0.35 \(\mu m\) CMOS technology. The proposed OTA greatly improves DC gain, GBW and slew rate concurrently by employing and integrating linear-nonlinear adaptive current mirror and cross-pair together. The high-resolution, fast speed OTA, especially minimum in settling time, can be used in switch-capacitor filter application.

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