A wide input voltage range level shifter circuit for extremely low-voltage digital LSIs

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Abstract: In this paper, we propose a level shifter circuit capable of handling a wide input voltage range. The circuit is based on a conventional two-stage comparator, and has a distinctive feature in that it operates a current amplification scheme for ultra low-power operation. The proposed circuit can convert low-voltage input digital signals into high-voltage output digital signals. The circuit achieves low power dissipation because it dissipates operating current only when the input signals change. Measurement results demonstrated that the circuit can convert low voltage input signals of 0.4 V into 3 V output signals. The power dissipation was 0.15 μW at 0.4-V and 10-kHz input pulse.

Keywords: level shifter, subthreshold, low power dissipation

Classification: Integrated circuits

References

1 Introduction

In recent studies, subthreshold digital LSIs, which are operated with supply voltage lower than the threshold voltage of a MOSFET, have attracted much attention to realize ultra-low power dissipation [1]. To achieve these LSIs, several studies have been carried out. However, a big issue is in a level shifter circuit design [2]. In this paper, we herein propose a compact level shifter circuit suitable for extremely low-voltage digital LSIs.

In low-voltage LSI systems, the subthreshold digital LSIs will be implemented with conventional circuits that are operated at a high supply voltage. Therefore, level shifter circuits are required to communicate with other circuits correctly. Moreover, they are also required when LSI designers have to test the functionality of the low-voltage subthreshold digital circuits. However, the communications and function tests become difficult when the conventional level shifter circuits are used because the supply voltage of the subthreshold digital circuits is below 0.5 V and that of peripheral circuits is still high (e.g., the supply voltage of I/O (input/output) peripheral circuits is 3.3 V). This is because the drive current of the low-voltage circuit significantly lowers as the supply voltage reduces and the conventional level shifter cannot convert input signals into high output signals. To mitigate this problem, several level shifters and remedies have been investigated [3, 4, 5, 6]. For example, increasing the drive current of the level shifters by enlarging the transistor channel width and multi-stage level shifters or inverters with plural supply voltages have been used. However, because these circuits still depend on the supply voltage difference and the circuit configuration becomes complex, the problem discussed above has basically not been solved.

To solve this problem, in this paper, we propose a level shifter circuit capable of handling a wide input voltage range. The proposed circuit can convert extremely low-voltage signals into high-voltage signals. The circuit is based on a conventional two-stage comparator circuit, and has a distinctive feature in its current amplification circuit. This paper is organized as follows: Section 2 briefly summarizes the problem in a conventional level shifter circuit and presents the operation principle of the proposed circuit, Sect. 3 shows the experimental results with a fabricated prototype chip, and Sect. 4 concludes the paper.

2 Level shifter circuit

Figure 1 (a) shows a conventional level shifter circuit. The circuit consists of cross-coupled pMOSFETs (MP1 and MP2) and two nMOSFETs (MN1 and MN2) driven by the complementary input signals of IN and INB. The circuit, however, has critical problems when the voltage difference between low supply voltage $V_{DDL}$ and high supply voltage $V_{DDH}$ becomes large.

When input logic signals of IN and INB are Low and High, MN1 and MN2 are Off and On, respectively. Then MN2 pulls down OUT and MP1 becomes On. Because OUTB increases to $V_{DDH}$, MP2 turns off and OUT decreases at GND level.
Fig. 1. (a) Conventional level shifter, (b) proposed level shifter, and (c) timing diagram for current amplification.

Note that the node voltage of OUT is determined by the drive currents of pull-up transistor MP2 and pull-down transistor MN2. Therefore, if the drive current of MP2 is larger than that of MN2, the node OUT cannot be discharged. Moreover, when we consider the case of subthreshold digital LSIs, because the on-current in MN2 becomes quite low, the drive currents of nMOSFETs will be significantly smaller than that of pMOSFET, which operates in the strong inversion region. Thus the nodes OUT and OUTB cannot be changed. Several level shifter circuits have been proposed to overcome the above problems [3, 4, 5, 6]. However, because these circuits are based on the cross-coupled circuit, they cannot solve the problems.

Figure 1 (b) shows the level shifter circuit we propose. The circuit consists of a current amplification circuit and a level shifting circuit. The complementary input signals of IN and INB are applied to both circuits.

The level shifting circuit is based on a conventional two-stage comparator circuit, as shown on the right in Fig. 1 (b). In the conventional design, it requires a current reference to operate steadily. However, because the current reference circuit dissipates static current and increases power dissipation, it cannot be used in our design. Therefore, we developed a current amplification circuit technique in which the current flowing in the circuit is amplified only when the input signals change.

The current amplification circuit is shown on the left in Fig. 1 (b). The circuit consists of two nMOSFETs (MN1 and MN2) connected in series and monitors the complementary input signals. Figure 1 (c) shows a timing diagram for the current amplification. When two input signals change, the time when both input signals are High exists as shown in Fig. 1 (c). By monitoring the period with two nMOSFETs in the current amplification circuit, the operating current $I$ for the level shifting circuit is supplied until one of the signals becomes Low. A maximum value of the amplified current is determined by $V_{DDL}$ and the delay time for the level shifting depends on the
current. When the input signals do not change, the current amplification circuit does not supply the current \( I \), and the power dissipation of the circuit can be minimized. Therefore, the proposed circuit achieves low-power dissipation. Moreover, after the voltage transition period, the node voltage of OUT is kept at stable voltage, i.e. \( V_{DDH} \) or GND. This is because OUT is charged or discharged with quite low leakage current in this period. The current cannot change the logic level of OUT.

Because the operation of the level shifting circuit is not symmetrical, the rise- and fall-times differ. Therefore, the duty ratio of output signal is changed when the input signal frequency is high. The rise- and fall-times depend on both the amplification current and gate voltage \( V_B \) of MN5.

### 3 Results

#### 3.1 Simulation

The performance of the proposed circuit was evaluated by using SPICE with a set of 0.35-\( \mu \)m CMOS parameters. \( V_{DDL} \) was set to 0.4–0.7 V and \( V_{DDH} \) was set to 3 V.

Figure 2 (a), (b), and (c) show simulated waveforms of the proposed level shifter circuit. The amplitude and frequency of the input signal were set at 0.4 V and 10 kHz, respectively. As shown in Fig. 2 (a), the 0.4-V input signal was converted into the 3-V output signal. Figure 2 (b) shows the current flowing through the current amplification circuit. As shown in the figure, when IN changed from Low to High, IN and INB had a period when both signals had high voltage, and then the amplified current was supplied to the level shifting circuit. However, when IN changed from High to Low, the period did not exist. This is because, in the process we used, pMOSFETs have a larger threshold voltage than nMOSFETs. Therefore, the rise transition time became larger than the fall transition time, and the period did not exist. However, the output voltage can change from High to Low correctly. This is because, thanks to the pMOSFET-input stage configuration of the level shifting circuit, the output voltage \( V_B \) of the first stage had enough voltage to pull down the output voltage when IN became Low. Therefore, the circuit could convert the 0.4-V input signals into the 3-V output signals. Figure 2 (c) shows the node voltages \( V_A \) and \( V_B \) in the level shifting circuit. As shown in Fig. 2 (a), (b), and (c), when the input signals did not change, the current was not supplied. \( V_A \) was slightly smaller than \( V_{DDH} \) and \( V_B \) was kept constant, near 1 V or GND. Therefore, the circuit operated correctly.

Figure 2 (d) shows the simulated delay and power dissipation of level shifters as a function of \( V_{DDL} \) at 1-kHz input pulse. We compared the performances both of the proposed and conventional circuits shown in Fig. 1 (a). Note that the delay was defined as the period when the input voltage signal was converted into the high output voltage signal. In the conventional circuit, as \( V_{DDL} \) decreases, the delay and power dissipation increase exponentially. This can be understood as follows. By decreasing \( V_{DDL} \), the delay increases exponentially because the drive current decreases exponentially. At
Fig. 2. (a) Input and output signals, (b) current flowing in current amplification circuit, and (c) node voltages $V_A$ and $V_B$ in level shifting circuit at 10-kHz input pulse. (d) Delay and power of level shifters as function of $V_{DDL}$ at 1-kHz input pulse.

Table I. Rise- and fall-times ($\tau_{\text{rise}}$ and $\tau_{\text{fall}}$) at different $V_{DDL}$.

<table>
<thead>
<tr>
<th>$V_{DDL}$ (V)</th>
<th>0.4</th>
<th>0.5</th>
<th>0.6</th>
<th>0.7</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\tau_{\text{rise}}$ ($\mu$s)</td>
<td>20.1</td>
<td>1.69</td>
<td>0.237</td>
<td>0.233</td>
</tr>
<tr>
<td>$\tau_{\text{fall}}$ ($\mu$s)</td>
<td>5.53</td>
<td>1.13</td>
<td>0.754</td>
<td>0.694</td>
</tr>
</tbody>
</table>

the same time, because input signals also require a long time for the signal transition, short current of the circuit increased. When $V_{DDL}$ was lower than about 0.54 V, the conventional circuit could not convert the low voltage signal into the 3-V signal. This was because the drive current of pull-down transistor decreased as the supply voltage $V_{DDL}$ decreased. The drive current below 0.54 V cannot change the output voltage as discussed above.

On the other hand, the proposed circuit can operate correctly below 0.54 V. Moreover, the proposed level shifter can convert the 0.4-V signal into the 3-V signal because both the drive currents in pull-up and pull-down transistors depend on the amplified current through the current amplification circuit. In the voltage range from 0.6 V to 0.7 V, the delay in the proposed circuit was independent of $V_{DDL}$. This is because the transistors in the current amplification circuit operated in the strong-inversion region and the dependence of the amplified current on $V_{DDL}$ became small. As $V_{DDL}$ decreased, the delay in the proposed level shifter increased exponentially because the delay depended on the amplified current, and in subthreshold bias conditions, the amplified current decreased exponentially as the $V_{DDL}$ decreased. Interestingly, as shown in Fig. 2 (d), the power of the proposed circuit scarcely depended on the change in $V_{DDL}$ and was almost constant. This is because, as $V_{DDL}$ decreased, the amplified current decreased exponentially while the period in which the current flows increased exponentially. As a result, the power dissipation of the circuit became constant. Table I shows the rise-
Fig. 3. (a) Chip micrograph (Chip area : 1850 $\mu$m$^2$). (b) Measured waveforms of our level shifter at 10-kHz input pulse. (c) Shmoo plots. (d) Measured power dissipations as function of $V_{DDL}$ at input frequencies of 0.1, 1, and 10 kHz.

and fall-times ($\tau_{\text{rise}}$ and $\tau_{\text{fall}}$) at different $V_{DDL}$s. As $V_{DDL}$ decreased, both the times increased exponentially because they depend on the amplified current as discussed in Sect. 2. The rise-time was longer at low $V_{DDL}$ than the fall-time because of asymmetrical transition of OUT.

3.2 Experimental

We fabricated a prototype chip using a 0.35-$\mu$m, 2-poly, 4-metal standard CMOS process. Figure 3(a) shows a micrograph of our prototype chip. The area was 1850 $\mu$m$^2$. $V_{DDH}$ was set to 3 V.

Figure 3(b) shows measured input and output waveforms of the level shifter at 10 kHz frequency. The circuit converted the 0.4-V signal into the 3-V signal.

Figure 3(c) shows the shmoo plot for the proposed level shifter operating frequency as a function of $V_{DDL}$. The maximum operating frequency increased exponentially as $V_{DDL}$ increased in the range of 0.4 to 0.64 V because the current flowing through the current amplification circuit increased exponentially as $V_{DDL}$ increased. With a voltage higher than 0.64 V, the operating frequency increased gradually with $V_{DDL}$ because the amplified current also increased in the same manner. These results corresponded with the simulation results shown in Fig. 2(d).

Figure 3(d) shows the measured power dissipations as a function of $V_{DDL}$ at the different input pulse frequencies of 0.1, 1, and 10 kHz. At the fixed pulse frequency, the power dissipations of the proposed level shifters were independent of $V_{DDL}$ same as with the simulation result in Fig. 2(d). The
power dissipation of the level shifter was extremely low, 0.15 μW at the input frequency of 10 kHz.

4 Conclusion

We proposed a level shifter for extremely low-voltage digital LSIs. The circuit can convert low input digital signals into high output digital signals and achieve low-power operation because it dissipates current only when the input signal changes. We fabricated a prototype chip using a 0.35-μm CMOS process, and demonstrated its operation by measurements. The circuit converted the 0.4-V input signal into the 3-V output signal. The power dissipation was 0.15 μW at 0.4-V and 10-kHz input pulse.

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