A fast and high efficiency buck converter with Switch-On-Demand Modulator for wide load range applications

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Abstract: This paper presents a buck converter with a switch-on-demand modulator (SOM) for achieving a fast transient response, small voltage ripple, and high power efficiency over a wide load range. Switching power MOS on or off depending on the energy demand of the load circuit results in a hybrid operation of pulse width modulation (PWM) and pulse frequency modulation (PFM). The proposed buck converter uses 90 nm CMOS process and can achieve a transient response time of less than 2 μ s and a voltage ripple of 18 mV at a load current range of 10 mA~500 mA with a power efficiency above 88%.

Keywords: buck converter, fast transient, wide load range

Classification: Integrated circuits

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1 Introduction

A high power efficiency buck converter is commonly required in many types of portable devices for extending the battery life. In buck converter designs, power losses come mainly from conduction losses with a heavy load while switching losses dominate with a light load [1]. To improve power efficiency over a wide load range, converters usually hop alternatively between PWM mode and PFM mode [2, 3, 4] for heavy and light load conditions, respectively. However, not only does the converter require different control blocks, the mode decision circuit should also be developed to precisely change the operation mode. As a result, the converter is complicated and incurs significant voltage variation during changes in the operation mode. Furthermore, a larger voltage ripple is induced in PFM mode because a large enough peak inductor current is set to improve the power efficiency [3].

In this paper, we propose the concept of a switch-on-demand modulator (SOM) for a buck converter to immediately switch power MOS on or off, depending on the energy demand of the load circuit. The SOM can achieve a hybrid operation of PFM and PWM without mode detection/change, allowing the buck converter with the proposed SOM to achieve a fast transient response and a small voltage ripple whilst improving power efficiency over a wide load range.

2 Design concepts

The conceptual waveforms of the load current (I_{Load}), inductor current (I_L), and the switching pulse of power MOS (V_G) generated by our proposed SOM are illustrated in Fig. 1. Also the inductor current ($I_{L,[3]}$) and the switching pulse of power MOS ($V_{G,[3]}$) generated by the dual mode converter proposed in [3] are illustrated in Fig. 1 for comparison. Consider that the highest switching frequency ($f_{s,max}$) of our proposed buck converter is limited by the

Fig. 1. A design concept of the proposed switch-on-demand modulator.

external inductor and capacitor, which are low-cost and prevalent. In the case of a gradually changing load current from a heavy load to light load, the on-time of power MOS (T_{ON}) is also gradually reduced towards a minimized value. The duty cycle (D) of the switching pulse of power MOS is defined in Eq. (1) where T_S , I_{Load} , R_{Load} , V_{out} and V_{in} represents the period of one switching cycle, load current, equivalent resistance of load circuit, regulated output, and input supply voltage, respectively.

$$\text{Duty}(D) = \frac{T_{ON}}{T_S} = \frac{V_{out}}{V_{in}} = \frac{I_{Load}R_{Load}}{V_{in}} \quad (1)$$

At the moment that the on-time of power MOS approaches the minimum value, the energy demand of the load circuit is relatively low, and hence the load current is also relatively low. Conduction losses become non-dominant as compared with switching losses, and the power MOS doesn't need to be switched on during each cycle to provide energy. Thus, the switching pulse generated by the SOM will appear to be "random". If the load circuit doesn't demand energy, the power MOS is switched off during the entire switching cycle to reduce switching losses. Otherwise, the power MOS is switched on with an appropriate T_{ON} , which was defined in Eq. (1) to adaptively provide sufficient peak current to the inductor (I_{L_peak}) and keep the output ripple small. The resulting I_{L_peak} of our proposed SOM is defined in Eq. (2) where L represents the inductance. As a result, the equivalent switching frequency (f_s) decreases and approaches the switching frequency of the PFM mode, as defined in [3]. The same methodology can be adapted for the case of a changing load current from a light load to a heavy load.

$$I_{L_peak} = \frac{T_{ON} \cdot (V_{in} - V_{out})}{L} \quad (2)$$

If the load current suddenly increases dramatically, as shown in Fig. 1, the proposed SOM will switch power MOS on immediately and last for many switching cycles until it can provide enough energy (shown in V_G of Fig. 1) while the dual mode converter [3] changes the operating mode from PFM to PWM and increase the inductor current ($I_{L,[3]}$) gradually. After the instantaneous energy requirement is supplied, the SOM will switch the power MOS at the frequency $f_{s,max}$, with the duty cycle defined in Eq. (1) to reduce conduction losses. In the case of suddenly decreasing load current dramatically, the SOM will switch off power MOS in the subsequent switching cycles until the provided energy is insufficient while [3] changes the operating mode from PWM to PFM after several PWM cycles. Therefore, the buck converter with our proposed SOM can achieve a fast transient response and a small voltage ripple with improved power efficiency for applications requiring a wide load range.

3 Circuit implementations

A current-mode buck converter has been designed, adopting the proposed SOM. A detailed block diagram is shown in Fig. 2(a) while the operating waveforms are shown in Fig. 2(b). The inductor current is sensed as a

Fig. 2. A current mode buck converter with the proposed SOM: (a) Block Diagrams; (b) Operating Waveforms.

voltage form (V_{SEN}), and is to be superposed on the periodic ramp waveform (V_{Ramp}) to avoid subharmonic oscillations [5]. The resulting summation signal (V_{CCS}) is then compared to the output of the error amplifier (V_{ea}), resulting in a comparison voltage (V_C). A clock signal (CLK) generated by the clock and ramp generator appears periodically at the highest switching frequency ($f_{s,max}$). If the CLK signal becomes high and V_C becomes low to demand energy, as shown at ① in Fig. 2 (b), the power MOS is switched on by resetting the SR latch of the switching pulse generator of the SOM. If the CLK signal becomes high and V_C stays high to represent sufficient energy transmitted, as shown at ③ in Fig. 2 (b), the power MOS is kept off without resetting the SR latch of the switching pulse generator. When the power MOS is on, V_{ea} gradually decreases, and V_{CCS} sharply increases. After the voltage level of V_{CCS} reaches V_{ea} , V_C will become high to switch off power MOS by setting the SR latch of the switching pulse generator shown at ② in Fig. 2 (b). The proposed switching pulse generator of SOM shown in Fig. 2 (a) is designed to have a higher priority on the V_C signal, which

is the set operation of the SR latch. The buck converter with the proposed SOM can thus switch off power MOS during an entire switching cycle to save switching power losses after it has provided enough energy to the load circuit. Furthermore, the proposed buck converter checks the energy demand of the load circuit during every switching cycle and can react immediately against load transients. Therefore, the proposed design will achieve a fast transient response and an accurate output voltage while improving power efficiency over a wide load range.

Fig. 3. Performance evaluation results: (a) Simulated waveforms of the output voltage and voltage ripple ($I_{Load} = 10\text{ mA} \sim 500\text{ mA}$); (b) Simulated power efficiency ($V_{in}/V_{out} = 3.3\text{ V}/1.8\text{ V}$).

4 Performance evaluations

The buck converter with the proposed SOM shown in Fig. 2(a) was designed using the 90 nm CMOS process to verify its feasibility. The input/output voltages were 3.3 V/1.8 V and the off-chip inductor L and capacitor C_L were selected as 4.7 μ H and 10 μ F, respectively. The $f_{s,\max}$ was chosen as 1 MHz. Fig. 3(a) shows the output transient response for the case of a load range from 500 mA to 10 mA, we also zoom in on the transient responses of overshoot/undershoot on the top of Fig. 3(a). The simulated overshoot/undershoot voltages ($\Delta V_{o+}/\Delta V_{o-}$) and the corresponding response times (T_{r+}/T_{r-}) were 58.78 mV/51.6 mV and 1.2 μ s/2 μ s. As compared with various previous works, e.g. 130 mV/66.5 mV and 28 μ s/10 μ s reported in [3], this result verifies that the proposed design has a better load transient response. Furthermore, the output ripple was smaller than 18 mV. As compared with 25 mV reported in [3], the proposed design guarantees an accurate, regulated output. Fig. 3(b) shows that the buck converter with the proposed SOM can boost efficiency by up to 12.03% as compared with the redesigned PWM buck converter [5] using a same process.

5 Conclusion

A new switch-on-demand modulator based buck converter is proposed to enhance the transient response while improve the power efficiency for applications requiring a wide load range. The proposed converter can achieve a power efficiency improvement of 12.03% at loads of 10 mA~500 mA. Meanwhile, the overshoot/undershoot was only 58.78 mV/51.6 mV with a response time of 1.2 μ s/2 μ s for the load transient, and the ripple voltage was smaller than 18 mV.

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