A simple curvature-compensated technique for CMOS bandgap voltage reference

Jin Wu\(^{1b)}\), Ning Qu\(^{1a)}\), Weidong Nie\(^2\), and Hao Li\(^1\)

\(^1\) The Southeast University, Wuxi, China
\(^2\) School of Information, Jiangnan University, Wuxi, China

a) quning2005@163.com
b) jwu@seu.edu.cn

Abstract: A simple high-order curvature-compensated technique for CMOS bandgap voltage reference (BVR) is presented and its advantage over the conventional ones is that this technique needs no extra circuitry for curvature compensation. The experimental prototype circuit is fabricated in CSMC 0.18 \(\mu\)m CMOS process and occupies an area of 0.053 mm\(^2\). A temperature coefficient (TC) of 10.1 ppm/\(^\circ\)C is achieved with temperature ranging from \(-40^\circ\)C to 120\(^\circ\)C under 3 V power supply. The line regulation of the output reference is only 0.85 mV/V.

Keywords: bandgap voltage reference, nonlinear compensation, temperature coefficient, mismatch current

Classification: Integrated circuits

References


1 Introduction

The bandgap voltage references (BVRs) are one of the most essential blocks
in many analog and digital systems e.g. A/D and D/A converters, voltage and current regulators, memory circuits, etc. The functionality of such systems is significantly influenced by the performance metrics of the used BVR from which the temperature stability is one of the most important. Concerning high precision requirements, it's critical to decrease the temperature coefficient (TC) of the BVRs as much as possible in a large temperature range, which depends on effective curvature-correction techniques. Much work has been done in BVRs with bipolar transistors to realize high-order temperature compensation [1, 2, 3, 4]. However, most of them require using high accurate amplifiers or additional structure for output voltage correction which increased the silicon area and power dissipation. In order to meet the goals of saving area and low power dissipation, it is desirable to use a simple circuit configuration avoiding an operational amplifier and many additional devices.

It is the purpose of this paper to present a simple voltage reference circuit with low TC by using a novel high-order curvature-compensated technique. Its key feature is that no operational amplifier or additional compensation devices are needed.

2 The Proposed new compensation technique

Figure 1 illustrates the proposed voltage reference circuit. It consists of a start-up circuit, a bias circuit and the bandgap reference core.

The startup circuit is needed to drive the circuits to the desired static operating condition and operates as following: before power on, the charge on capacitor $C_0$ is empty to provide a low potential. Along with the increasing of power supply, both PMOS transistors $P_1$ and $P_2$ turn on, the current of $P_2$ injects into the gate capacitor of NMOS transistors to startup the bandgap core, at the same time, current of $P_1$ start to charge $C_0$, driving the potential.

![Fig. 1. The proposed Bandgap voltage reference circuit.](image-url)
of $C_0$ gradually approaching to $V_{DD}$, which, in turn, turns off the startup circuit.

2.1 Principle of the first-order compensated BVR

As shown in Fig. 1, the bias circuit consists of NMOS transistors $NM_2$, $NM_3$, PMOS transistors $PM_6$ and $PM_7$, and bipolar transistors $Q_2$ and $Q_3$ with the same area. Consider the bandgap reference core, cascode current mirror composed of $PM_0$-$PM_5$ is introduced to enhance the transmission accuracy of the generated current and to improve the power supply rejection ratio (PSRR). A current proportional to absolute temperature (PTAT), $I_{PTAT}$, is generated when $V_A = V_B$, the source voltage of transistors $NM_0$ and $NM_1$, which is enforced by the voltage-clamping circuit composed of $NM_0$ and $NM_1$. The current $I_{PTAT}$ with random mismatch neglected can be presented as:

$$ I_{PTAT} = \frac{(V_{BE1} - V_{BE0})}{R_0} = \frac{\Delta V_{BE}}{R_0} = \frac{V_T \ln N}{R_0} $$

(1)

Where $N$ is the emitter-area ratio between $Q_0$ and $Q_1$, and $V_T$ is the thermal voltage. Capacitor $C_C$ in the circuit is added for the purpose of frequency compensation to make sure loop stability. In order to reduce random mismatch between $V_A$ and $V_B$, all transistors in the two dashed boxes as indicated in figure 1 are in the same size and carefully layout designed, respectively. $V_M$ equals to $V_N$ when $PM_3$ and $PM_7$, biased in the saturation region, are sized by the same current per unit $W/L$. The ideal current $I_{PTAT}$ is mirrored to the output branch to form linear-compensated BGR. The reference voltage ($V_{ref}$) is given by:

$$ V_{ref} = V_{BE4} + m \frac{R_2}{R_0} \Delta V_{BE} = V_{BE4} + (m \frac{R_2}{R_0} \ln N)V_T $$

(2)

Where $m$ is the current mirror ratio between $PM_5$ (or $PM_4$) and $PM_3$ (or $PM_2$). $R_2$ is the resistor in the output branch to form a PTAT voltage. Here, the accurate temperature characteristic of $V_{BE}$ is governed by the following expression:

$$ V_{BE}(T) = V_G(T) - [V_G(T_0) - V_{BE}(T_0)] \frac{T}{T_0} - (\gamma - \alpha)V_T \ln \left(\frac{T}{T_0}\right) $$

(3)

Where $T_0$ is the temperature at which the TC of the reference is zero, usually chosen to be near room temperature. $\gamma$ is a constant depending on doping level, and $\alpha$ is a constant depending on the temperature character of emitter current in BJT. $V_G$ is the bandgap voltage of silicon, and its temperature characteristic can be modeled to the following empirical equation:

$$ V_G(T) = V_G(T_0) + TC_1(V_G)(T - T_0) + \frac{1}{2}TC_2(V_G)(T - T_0)^2 $$

(4)

Where $V_G(T_0)$ is the silicon bandgap at $T_0$ K. $TC_1(V_G)$ and $TC_2(V_G)$ represent the first-order and the quadratic TC of $V_G$. Deriving from expressions (2)-(4) the optimally first-order compensated reference voltage ($V_{ref,1}$) when the linear term of temperature in $V_{BE}$ is fully cancelled can be expressed as:

$$ V_{ref,1}(T) = V_{G0} + \frac{1}{2}TC_2(V_G)T^2 + (\gamma - \alpha)V_T[1 - \ln \left(\frac{T}{T_0}\right)] $$

(5)
where $V_{G0}$ represents the ideal bandgap voltage with TC=0. Here, we define the remaining temperature-related nonlinear voltage in $V_{\text{ref,1}}$ as $V_{NL}$, that is, $V_{\text{ref,1}} = V_{G0} + V_{NL}$. To further improve the accuracy of the reference, high-order curvature compensation technique is necessary to compensate $V_{NL}$.

2.2 Principle of the proposed new compensation technique

For the symmetrical first-order bandgap reference, as described in section 2.1, we have $V_A = V_B$ and $V_M = V_N$ if there isn’t any mismatch current generated. However, if process variation considered, random mismatch between $V_A$ and $V_B$ or $V_M$ and $V_N$ are generated. If the normalized W/L ratios between PM$_3$ and PM$_7$ are modified artificially by the designer, a significant systematic mismatch between $V_M$ and $V_N$ is introduced. Then, a systematic mismatch current $\Delta I = I_1 - I_0$ due to channel modulation effect is generated between $I_1$ and $I_0$, which is far greater than the random quantity. Premising that $V_A \approx V_B$ is still valid without considering process random mismatch, the voltage $\Delta V_{BE}$ in Equation (1) is modified to:

$$\Delta V_{BE} = V_T \ln(N \frac{I_1}{I_0}) = V_T \ln N + V_T \ln \beta$$

(6)

Where $\beta = I_1/I_0$, $\ln \beta = \ln(I_1/I_0) = \ln[1 + (\Delta I/I_0)]$. On the mathematical principle of $\ln(1+x) \approx x$ while $x$ tends to zero, we can obtain $\ln \beta \approx \Delta I/I_0$ because $\Delta I$ is much less than $I_0$. Finally, the additional nonlinear voltage ($V_{NL,ADD}$) formed at the output branch can be given by:

$$V_{NL,ADD} = m \frac{R_2}{R_0} V_T \ln \beta = m \frac{R_2}{R_0} V_T \frac{\Delta I}{I_0} = m R_2 \frac{\Delta I}{\ln N}$$

(7)

Thus, owing to the factitious systematic mismatch compensation current, the reference voltage can be expressed as $V_{\text{ref,2}} = V_{G0} + V_{NL} + V_{NL,ADD}$.

Generally, adding nonlinear PTAT$^2$ (proportional to absolute temperature squared) term and TlnT term to cancel the curvature of $V_{BE}$ is widely used in published papers, which require additional devices and power dissipation. Fortunately, both quantity and polarity of $V_{NL,ADD}$ can be accurately defined through $\Delta I$, so $V_{NL,ADD}$ can be used as the compensation voltage to cancel out $V_{NL}$, improving the TC of the reference voltage. The temperature characteristic of $V_{NL,ADD}$, which is related to resistor $R_2$ and $\Delta I$, can be indicated concretely as:

$$V_{NL,ADD} = m \frac{\Delta I}{\ln N} R_2(T_0)[1 + TC_1(T - T_0) + TC_2(T - T_0)^2]$$

(8)

Where $TC_1$ and $TC_2$ are the first-order and second-order TC of $R_2$, respectively. Usually, $R_2$ is implemented by high-resistive poly resistor and has a negative $TC_1 = -0.97 \times 10^{-3}$ and positive $TC_2 = 1.85 \times 10^{-6}$ in CSMC 0.18 $\mu$m CMOS process. The needed high-order correction terms can be optimized by an appropriate value of $\Delta I$ and $R_2$. So, if $V_{NL}$ can be largely compensated by the configurable $V_{NL,ADD}$, a more temperature stable BVR is obtained.
2.3 Design issues

Precision voltage references are seriously degraded by any small variation in current due to device randomly mismatches, such as in the threshold of MOS transistors, the absolute values of $W$ and $L$, and sheet resistance of resistors, When placing the layout, the transistors in the two dashed boxes and resistors of $R_0$-$R_2$ should be matched completely to minimize the mismatch.

For the high-order compensated BVR, artificially systematic mismatch voltage between $V_M$ and $V_N$ is set at the level of a few hundred $mV$ or even larger, which result in a mismatch current between $I_0$ and $I_1$ at the level of dozens nA, then, variation at Vref is 1-3$mV$ when $R_2$ is a couple hundred kilo-ohm. Unfortunately, variation voltage at Vref caused by the random mismatch, $V_{NL_random}$, may reach to the level of dozens $mV$, which is an order of magnitude larger than systematic mismatch voltage. Therefore, trimming technique applied to $R_2$ is necessary so that an intentional trimmed voltage $V_{NL Trim}$ can be achieved and used to cancel out $V_{NL_random}$. It uses an simple on-chip 4-bits bidirectional nonlinear resistor trimming array with 16 tunable voltage levels, where the least significant trimmed voltage is 2.5$mV$ and the tolerable maximum trimmed voltage is 60$mV$. The practical TC will significantly exceed its theoretical values without trimming technique adopted.

![Fig. 2.](a) Chip micrograph of the BVR, (b) Simulation TC, (c) Measured TC and (d) Line regulation.

3 Experimental results and analysis

The proposed bandgap reference circuit in Fig. 1 is implemented in CSMC 0.18 $\mu m$ CMOS process. The chip micrograph is shown in fig.2(a) and the effective chip area is 0.053 mm$^2$, among which the trimmed resistors occupied...
approximately one third.

Twenty samples are measured. Fig. 2 (b) shows the simulation TC from $-40^\circ C$ to $125^\circ C$ with 3 V supply voltage is 4.6 ppm/$^\circ C$, while fig.2 (c) shows four curves of tested TC, the trimmed minimum TCs of the proposed BVR are 10.1 ppm/$^\circ C$(BVR1) and 15.5 ppm/$^\circ C$(BVR2) over the temperature range from $-40^\circ C$ to $120^\circ C$ under 3 V and 2.4 V power supply, respectively. That different power supplies lead to different TCs because random mismatch of the circuit under 3 V is smaller than that of 2.4 V. The maximum variation of the output voltage with 3 V and 2.4 V power supply in the temperature range of $-40^\circ C$-120$^\circ C$ are 3.2 mV and 5.3 mV, respectively, so the worst TCs among the twenty tested samples are 17.1 ppm/$^\circ C$(BVR3) and 28.2 ppm/$^\circ C$(BVR4).

Fig. 2 (d) shows that the variation in the output voltage of the BVR is only 1.7 mV when the power supply voltage changes from 2 V to 4 V, so the line regulation is 0.85 mV/V. The theoretical supply current of the BVR is 21.8 $\mu$A, while the tested result averaging from the twenty samples is 21 $\mu$A, where the minimum and the maximum value are 19.6 $\mu$A and 22.7 $\mu$A, respectively.

Table I. Comparisons of the curvature-corrected BVRs.

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<th>Process (μm)</th>
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<th>Ref.[2]</th>
<th>Ref.[3]</th>
<th>Ref.[4]</th>
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<td>CMOS 0.35</td>
<td>CMOS 0.6</td>
<td>CMOS 0.35</td>
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<td>Measured TC (ppm/$^\circ C$)</td>
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<td>5.3</td>
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<td>Temperature range ($^\circ C$)</td>
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<td>$20$–$100$</td>
<td>$0$–$100$</td>
<td>$5$–$95$</td>
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<tr>
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<td>/</td>
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<td>3.5</td>
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<tr>
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<td>55</td>
<td>23</td>
<td>16.6</td>
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<tr>
<td>Chip Area (mm$^2$)</td>
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4 Conclusion

A simple high-order curvature-compensated technique for CMOS BVR is presented and its advantage over the conventional ones is that no extra circuitry required for curvature compensation. The proposed BVR achieves TC of 10.1 ppm/$^\circ C$ at 3 V supply. Table I lists experimental performance comparison of some published state-of-art curvature compensated BVRs with our work. Comparison result shows that comparable TC in a larger TR is achieved by the proposed simple BVR. Moreover, the line regulation is better than the others. In a word, the experiment results show the validity and practicability of the proposed technology.

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