Compact three-way planar power divider using five-conductor coupled line

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Abstract: In this paper, a planar three-way power divider with compact size is presented using quarter-wave long five-conductor coupled line. It is analytically proved that the proposed structure allows the performance of three-way power dividers. Based on the derived equations and simulation, the three-way power divider is designed and measured at 2.0 GHz. The measurement shows excellent performance with insertion loss of 0.2 dB, and return loss and isolation better than 20 dB at a design frequency.

Keywords: power divider, coupled line, impedance matching, Wilkinson

Classification: Microwave and millimeter wave devices, circuits, and systems

References

1 Introduction

Power dividers are one of the essential components in the microwave circuits and systems. In a conventional \(N\)-way Wilkinson power divider, \(N\) quarter-wave long lines are required and they should be laid out sufficiently apart from each other to minimize electromagnetic couplings [1]. Therefore, it is difficult to design compact multi-way power dividers \((N > 2)\) in the planar form. In [2], three-way power divider was proposed using three of two-way power dividers, which solved the layout problem but still occupied large circuit area. Multi-conductor coupled lines were employed in [3] to implement three-way power divider, which effectively reduced the circuit area. However, the multi-conductor coupled line was not analyzed to prove that the structure could function as a power divider. Besides, the structure requires DC blocking capacitors at every port, since one end of each conductor line is connected to a port and the other end is grounded (therefore, each port is grounded at DC).

In this work, a new planar three-way power divider with compact size is presented using five-conductor coupled line which provides DC block characteristics to every port. In addition, a detailed analysis is performed to analytically verify the operation of the proposed structure and to help design of five-conductor coupled line. Then, the proposed power divider is designed based on the analysis and simulation. The measured three-way power divider shows good agreement with simulation with excellent performance.

2 Analysis of three-way power divider

Fig. 1 illustrates the proposed three-way power divider in a microstrip form. It consists of a quarter-wave long five-conductor coupled line and three isolation resistors \(R\). Two conductor lines (2, 4) are connected to port 1 \((P_1)\) at one ends with the other ends open-circuited. One ends of the other conductor lines (1, 3, 5) form the output ports with the other ends connected together. Therefore, there is no need of DC blocking capacitors at every port, which is attractive in a circuit design and fabrication. The coupled line is symmetric along the center conductor (3) as described in Fig. 1 (b) which shows the cross section of five-conductor coupled line in a microstrip form.

In order to prove that the proposed structure can allow the perfect operation of three-way power divider, the five-conductor coupled line is analyzed using admittance parameters or Y-parameters. For quarter-wave long symmetric five-conductor coupled line, the following relations hold for the currents and voltages at the terminal of each conductor line (refer to Fig. 1 (a) for the notation of currents and voltages) [4, 5]:

\[
\begin{align*}
I_{1a} &= j(Y_{11} V_{1b} + Y_{12} V_{2b}), & I_{1b} &= j(Y_{11} V_{1a} + Y_{12} V_{2a}) \\
I_{2a} &= j(Y_{12} V_{1b} + Y_{22} V_{2b} + Y_{23} V_{3b}), & I_{2b} &= j(Y_{12} V_{1a} + Y_{22} V_{2a} + Y_{23} V_{3a}) \\
I_{3a} &= j(Y_{23} V_{2b} + Y_{33} V_{3b} + Y_{23} V_{4b}), & I_{3b} &= j(Y_{23} V_{2a} + Y_{33} V_{3a} + Y_{23} V_{4a}) \\
I_{4a} &= j(Y_{23} V_{3b} + Y_{22} V_{4b} + Y_{12} V_{5b}), & I_{4b} &= j(Y_{23} V_{3a} + Y_{22} V_{4a} + Y_{12} V_{5a}) \\
I_{5a} &= j(Y_{12} V_{4b} + Y_{11} V_{5b}), & I_{5b} &= j(Y_{12} V_{4a} + Y_{11} V_{5a}),
\end{align*}
\]
where \( Y_{mn} \)'s are admittance parameters determined by capacitances and phase velocity \( v_p \) as follows:
\[
Y_{11} = v_p (C_{10} + C_{12}), \quad Y_{22} = v_p (C_{20} + C_{12} + C_{23}), \\
Y_{33} = v_p (C_{30} + 2C_{23}) \text{ and } Y_{12} = -v_p C_{12}, \quad Y_{23} = -v_p C_{23}.
\]
The capacitances are denoted in Fig. 1 (b), where \( C_{n0} (n = 1, 2, 3) \) represents self capacitance per unit length between each conductor line and ground, and \( C_{12} \) and \( C_{23} \) are mutual capacitances per unit length between two adjacent conductor lines. The mutual capacitance between non-adjacent conductor lines is ignored for simplicity of the analysis, which is a reasonable approximation [5, 6].

In order to determine the conditions for impedance matching at port 1, suppose that the power is injected into port 1 and is equally split into each output port. Then, the following relations are satisfied, considering the symmetry of the structure:
\[
V_{1a} = V_{3a} = V_{5a}, \quad V_{1b} = V_{3b} = V_{5b}, \quad V_{2a} = V_{4a}, \quad V_{2b} = V_{4b}, \quad I_{2a} = I_{4a}, \quad I_{2b} = I_{4b} = 0, \text{ and } I_{1a} = I_{3a} = I_{5a} = 0.
\]
Since output ports are terminated by a reference impedance \( Z_0 \), and isolation resistors are open-circuited in this excitation, it follows that \( V_{1b} = -Z_0 I_{1b}, \quad V_{3b} = -Z_0 I_{3b}, \text{ and } V_{5b} = -Z_0 I_{5b}. \) These relations can be solved with Eq. (1)–(5) to give the following conditions on Y-parameters:
\[
Y_{11} = Y_{33} \quad (6) \]
\[
Y_{12} = 2Y_{23} \quad (7)
\]
Substituting Eq. (6)–(7) into Eq. (2) yields another condition for impedance matching.
matching at port 1 as

\[ 3Y_{12} - \frac{2Y_{11}Y_{22}}{Y_{12}} = \sqrt{3}Y_0 \]  

(8)

Therefore, Y-parameters of the coupled line should satisfy Eq. (6)–(8) to achieve impedance matching at port 1. If these equations are substituted into Eq. (1)–(5), it can be easily found that

\[ \frac{V_1b}{V_{2a}} = \frac{V_3b}{V_{2a}} = \frac{V_5b}{V_{2a}} = -j/\sqrt{3}, \]

implying that input power is equally split into output ports without loss.

The conditions for impedance matching and isolation at output ports can be derived by analyzing the circuit with the power injected into port 2. In this excitation, it holds that

\[ V_{1a} = V_{3a} = V_{5a} = I_{1a} + I_{3a} + I_{5a} = 0, \quad I_{2b} = I_{4b} = 0, \]

and

\[ V_{2a} = V_{4a} = -(I_{2a} + I_{4a})Z_0. \]

Assuming the impedance matching at port 2 and isolation between output ports (that is, \( V_{3b} = V_{5b} = 0 \)), then KCL at port 2 yields

\[ V_{1b}/Z_0 = I_{1b} + 2V_{1b}/R. \]

The substitution of these relations into Eq. (1)–(5), the isolation resistance \( R \) is determined as

\[ R = 3Z_0 \]

(9)

By substituting Eq. (6)–(9) into Eq. (1)–(5), it is proved that impedance matching can be achieved at all output ports (including port 3).

In summary, Eq. (6)–(9) represent the conditions on which the proposed structure can satisfy the required performance of three-way power dividers, that is, no insertion loss from input to outputs, perfect impedance matching at all ports, and perfect isolation between output ports. In this section, it is proved by the analysis that the proposed structure can function as a perfect three-way power divider.

The Eq. (6)–(8) on Y-parameters can be converted to the relations between capacitances as follows:

\[ C_{12} = 2C_{23}, \quad C_{10} = C_{30}, \quad \text{and} \quad C_{20} = C_{12} \left( \sqrt{3}C_0 - 3C_{10} \right)/(2(C_{10} + C_{12})), \]

where \( C_0 = Y_0/v_p \). These relations can be effectively used to initially determine the dimension of the coupled line, even though there exist many combinations of capacitances satisfying these relations. Then, the electromagnetic simulation can be performed to finalize the dimension.

### 3 Measurement of three-way power divider

In order to verify the analysis, the proposed three-way power divider was fabricated using 30 mil-thick FR4 substrate with dielectric constant of 4.5. The five-conductor coupled line was designed based on the analysis and optimized by using commercial electromagnetic simulator (ADS Momentum) as follows:

\[ W_1 = 0.26 \text{ mm}, \quad W_2 = W_3 = 0.4 \text{ mm}, \quad S_1 = 0.07 \text{ mm}, \quad \text{and} \quad S_2 = 0.17 \text{ mm}. \]

The center frequency is 2.0 GHz, and the length is 19.4 mm. Fig. 2 shows the fabricated three-way power divider. SMA connectors are attached at each port for the S-parameter measurement. This photograph demonstrates that the proposed three-way power divider using five-conductor coupled line can be very compact compared to the conventional Wilkinson coupler.
Fig. 2. Fabricated planar three-way power divider.

Fig. 3. Measured (solid line) and simulated performance (dotted line) of the power divider. (a) Insertion loss. (b) Return loss. (c) Isolation. (d) Phase delay.

The measurement results are presented in Fig. 3 along with simulated performance. They are in a good agreement. The measured insertion losses ($S_{21}$, $S_{41}$ and $S_{31}$) are less than 5.0 dB which corresponds to only 0.2 dB loss compared to the ideal value of 4.8 dB for three-way power divider. The return losses ($S_{11}$, $S_{22}$, $S_{44}$ and $S_{33}$) are better than 20 dB as shown in Fig. 3 (b). The input return loss ($S_{11}$) shows narrower bandwidth than the output return losses. It is because the input matching is achieved by quarter-wave long
transmission line only with high impedance transformation ratio. On the contrary, the isolation resistors are used with transmission lines for the output impedance matching, which reduces the quality factor of the impedance matching circuit [7]. Therefore, the broad bandwidth can be obtained in the output return losses. The power divider shows an excellent isolation performance ($S_{32}$, $S_{43}$ and $S_{42}$) better than 20 dB at a design frequency as shown in Fig. 3 (c). Fig. 3 (d) shows the measured phase of $S_{21}$ and $S_{31}$, indicating the phase delay difference of only 1.3 degree between output ports at 2.0 GHz. The phase delay of $S_{41}$ is omitted for the better readability of the figure, since it is almost same as that of $S_{21}$. It is worthwhile to note that the measurement results about port 2 and port 4 are very similar since they are symmetric in the layout. The simulation results about port 4 are omitted in Fig. 3 by this reason.

4 Conclusion

In this paper, planar three-way power divider with compact size was presented using five-conductor coupled line. It was verified by the analysis that the proposed structure could present the required performance of power divider. The designed power divider showed excellent performance in the insertion loss, return loss and isolation. The proposed structure can be easily extended for the planar $N$-way power divider with $N > 3$ by using more conductors in the coupled line. Therefore, this work demonstrates that the power divider using multi-conductor coupled lines can be effectively applied to various microwave circuits and systems.

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