DC gain enhancement method for recycling folded cascode amplifier in deep submicron CMOS technology

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Abstract: A DC gain enhanced recycling folded cascode amplifier with a new positive feedback output stage is presented. The proposed amplifier using positive feedback to cancel the output conductance allows DC gain to be enhanced without affecting the bandwidth of the amplifier. The proposed amplifier was implemented in SMIC standard 65 nm CMOS process. Simulation results show that a DC gain enhancement of 35 dB is achieved without limiting the bandwidth.

Keywords: DC gain enhancement, recycling folded cascode amplifier, positive feedback

Classification: Integrated circuits

References


1 Introduction

High gain and high speed are two most important properties of the operational transconductance amplifier (OTA) [1, 2]. Recently, the recycling folded cascode (RFC) amplifier has gained preference over other structure amplifiers.
owing to its improved gain-bandwidth (GBW) and DC gain [3]. However, as feature sizes decreased, especially in deep submicron CMOS technology, the transistor gain factor \( g_m r_o \) has also rapidly decreased [4]. Currently, for 65 nm CMOS technology, the gain factor \( g_m r_o \) is on the order of only 3-6, which leads to a significant decreased DC gain.

In this paper, a DC gain improved recycling folded cascode amplifier with a new positive feedback output stage is presented. Positive feedback generates a negative conductance and thus cancels the output conductance of the amplifier. In this way, a very high DC gain can be obtained. The newly proposed amplifier does not introduce any supplementary internal nodes and consequently the frequency performance is identical to the traditional RFC. The rest of the paper is organized as follows. In section 2 the proposed DC gain improved amplifier is analyzed. Simulation results are indicated in section 3 and section 4 concludes the paper.

2 Architecture of the proposed IRFC amplifier

2.1 Basic topology

In the conventional RFC structure, the input drivers are split in half to produce transistors \( P1a(b) \) and \( P2a(b) \). Also, the cross-over connections of current mirrors \( N1 : N5 \) and \( N2 : N6 \) with a ratio of \( K : 1 \) ensure that the small signal current is amplified \( K \) times. The enhanced transconductance and increased output impedance lead to a boost in DC gain. However, in deep submicron CMOS technology, the DC gain of the RFC has rapidly decreased, which is due to the smaller transistor gain factor \( g_m r_o \).

To enhance the DC gain of the conventional RFC, a DC gain improved recycling folded cascode amplifier (IRFC) is proposed, which is shown in Fig. 1. The proposed amplifier is very similar to the conventional RFC configuration.

![Fig. 1. Architecture of DC gain improved recycling folded cascode amplifier (IRFC).](image)
except the load, which is implemented by two cross-coupled simple current mirrors ($P_8$, $P_{10}$ and $P_9$, $P_{11}$) cascoded by transistors $P_5$ and $P_6$.

2.2 Small signal analysis

The voltage gain transfer function of the amplifier is obtained as:

$$A_v = G_m \cdot R_{out}$$  \hspace{1cm} (1)

Ignoring the bulk effect for simplicity, the IRFC has a small signal equivalent circuit and the open loop DC gain of this amplifier, $A_v_{IRFC}$, can be described as follow:

$$A_v_{IRFC} = -(K+1)g_{mP1}/[g_{mN3}(g_{oP1}+g_{oN1}) + g_{oP5}(g_{mP8} - g_mP11+g_{oN11})]/g_{mN3}$$  \hspace{1cm} (2)

where $g_{mi}$ and $g_{oi}$ is the effective transconductance and output conductance of transistor $M_i$. Transistors $P_8$ and $P_9$ ($P_{10}$ and $P_{11}$) are identical. Eq. (2) indicates that the second part of the output resistance can become negative if $g_{mP11}$ is significantly larger than $g_{mP8}$. This negative resistance connected in parallel to the output node can be used to cancel the output conductance of amplifier. Assuming that $g_{mN3} = g_{mP5}$, $g_{oN3} = g_{oP5}$ and $g_{oP11} << g_{oP1,N1}$, the $A_v_{IRFC}$ can be written as:

$$A_v_{IRFC} = -(K+1)g_{mP1}/[g_{oN3}(g_{oP1}+g_{oN1} + g_{mP8} - g_mP11)]/g_{mN3}$$  \hspace{1cm} (3)

From Eq. (3), it can be seen that as $g_{mP11}$ approaches $g_{oP1} + g_{oN1} + g_{mP8}$, a theoretically infinite DC gain can be obtained. Eq. (3) can be implemented by proper design of the dimensions of transistors $P_8$ and $P_{11}$. The precision of the conductance cancellation depends essentially on the matching property of the transistors. The circuit may have a negative output resistance if the positive feedback is too strong. This leads to instability due to the right-half pole. To avoid the instability problem, some security margin should be conserved. The security margin can be determined by simulation.

2.3 Output swing and frequency performance

To maintain all transistors in Fig. 1 in saturation, the output voltage has to fulfill the following condition:

$$V_{out} \leq |V_{DD} - V_{SS} - 2V_{sat,P} - 2V_{sat,N} - V_{th,P}|$$  \hspace{1cm} (4)

Therefore the output swing of the IRFC is one $V_{th,P}$ less than that of the conventional RFC structure.

Also, the gain enhancement does not have any influence on the frequency performance because no supplementary node is added. The cross-coupled current mirror structure makes the parasitic capacitor larger than the RFC structure. However, a zero at approximately the same position is also created, so the effect of this pole is cancelled out. The dominant pole of the proposed IRFC is determined by the load capacitor and the first non-dominant pole depends on the parasitic capacitor at folded node as in the conventional RFC configuration.
3 Simulation results

Two amplifiers, RFC and IRFC, are designed with the same power in SMIC standard 65 nm CMOS process, using a single supply of 1.2 V. The amplifiers were biased with the same circuitry and had the same common-mode feedback

Table I. Performance summary of RFC and IRFC.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conventional RFC</th>
<th>Proposed IRFC</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Gain (dB)</td>
<td>51.9</td>
<td>87.6</td>
</tr>
<tr>
<td>GBW (MHz)</td>
<td>121</td>
<td>121</td>
</tr>
<tr>
<td>Phase margin (deg)</td>
<td>79.2</td>
<td>78.6</td>
</tr>
<tr>
<td>Power (uA)</td>
<td>245</td>
<td>245</td>
</tr>
<tr>
<td>Supply Voltage (V)</td>
<td>1.2</td>
<td>1.2</td>
</tr>
<tr>
<td>Output Swing (V)</td>
<td>0.86</td>
<td>0.58</td>
</tr>
</tbody>
</table>

Fig. 2. Open loop AC response showing variations of IRFC with process corners.
(CMFB) implementation. Both the RFC and IRFC are loaded with 2.5 pF capacitor at each branch. For the IRFC, the positive feedback is introduced by taking the same $L$ and different $W$ for $P_8$, $P_9$ and $P_{10}$, $P_{11}$. Table I lists the specifications of the conventional RFC and the proposed IRFC. It shows that the DC gain of the RFC and the IRFC is 51.9 dB and 87.6 dB, respectively. The DC gain of the IRFC increased 35.7 dB compared to the conventional RFC. Considering the mismatch effect to the proposed IRFC, Monte Carlo simulation has been done and results show that the reduction of DC gain is less than 1.5 dB. On the other hand, variations of the proposed IRFC with process corners is shown in Fig. 2, which shows a reduction of 2 dB in DC gain in FF corner and an improvement of 1.3 dB in SS corner. Also, the proposed IRFC shows slight variations in SF and FS corners. Also, both the GBW of the RFC and the IRFC are 121 MHz, which shows that the GBW of the IRFC is not limited. Finally, the output swing of the IRFC reduces a $V_{th,p}$ owing to the positive feedback pairs.

## 4 Conclusion

A DC gain enhanced recycling folded cascode amplifier with a new positive feedback output stage is presented. The proposed amplifier was implemented in SMIC standard 65 nm CMOS process. Simulation results show that the DC gain of the IRFC improved 35 dB without limiting the bandwidth compared to the RFC.