Selective etching of HfN gate electrode for HfN/HfSiON gate stack in-situ formations

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Abstract: In order to fabricate metal gate/high-k gate stacks utilizing ECR sputtering, selective etching of HfN gate electrodes was investigated. It was found that etching rates of HfN gate electrodes at room temperature were 2.9 and 0.23 nm/s for DHF (1%) and the mixed solution of HF:H₂O₂:H₂O = 1:2:40, respectively. In addition, the etching selectivity for HfN/HfSiON was relatively high, such as the ratio of 65 which was 3 times higher than that of DHF (1%) by the mixed solution. After the in-situ formation of HfN/HfSiON layers on p-Si(100) and post deposition annealing (PDA), patterning of HfN was carried out utilizing the selective etching process. In case the PDA of 800°C/15 s, the MOS diodes were found to be successfully fabricated, and the equivalent oxide thickness (EOT) of 0.56 nm, and the leakage current at V_{FB}-1 V of 1.3 A/cm² were obtained.

Keywords: HfN, HfSiON, MG/HK, ECR plasma sputtering

Classification: Electronic materials, semiconductor materials

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1 Introduction

For the scaling down of CMOS technology, metal gate/high- κ (MG/HK) gate structures, which have a high permittivity (high- κ) material as a gate insulator and metal as a gate electrode, have been widely studied, instead of conventional poly-Si/SiON gate stack structures [1, 2, 3, 4, 5]. HfO₂, which is one of the most promising high- κ materials, has problems in thermal stability such as crystallization at high temperature process and formation of an interfacial low permittivity layer (IL) at HfO₂/Si interfaces [6]. In addition, the chemical vapor deposition (CVD) is a generally used method for high- κ deposition; however, it still has some problems in obtaining a small equivalent oxide thickness (EOT), such as less than 1 nm, because contamination by residues of precursor source gases and pin-hall formation by island shaped growth generally degrade film qualities such as the leakage properties of films [7, 8]. Therefore, we have studied the formation of high permittivity HfSiON thin film with higher thermal stability than HfO₂ by incorporation of Si and N atoms utilizing ECR sputtering method [9]. The ECR sputtering method realizes to form a high quality thin film by low damage plasma. Moreover, we have investigated HfN gate electrode, which has a higher thermal stability than widely studied TiN and TaN. Thus, in-situ formation of HfN/HfSiON formed by HfSiON deposition followed by in-situ HfN deposi-

tion has been studied [10]. In this paper, a condition of selective etching for HfN gate electrodes in HfN/HfSiON gate stack structures was investigated. In addition, characteristics of metal-insulator-semiconductor (MIS) diodes formed by in-situ process were evaluated.

2 Experimental procedure

The p-Si(100) wafers were chemically cleaned followed by immersion in H₂O₂ to form chemical oxide (C'O) layers (0.7 nm). Then, 1 nm-thick HfN (HfN:N $\cong$ 1:1) was deposited by ECR sputtering (0.19 Pa; Ar/N₂: 25/1 sccm; μ -wave: 2.45 GHz; μ -wave/RF power: 500/500 W) at room temperature followed by the in-situ oxidation of HfN to form HfON (0.18 Pa; Ar/O₂: 20/8 sccm; μ -wave: 300 W) for 3 s. After the in-situ oxidation, HfN (40 nm) was in-situ deposited (Ar/N₂: 20/0.8 sccm; μ -wave/RF power: 400/500 W). PDA was performed by silicon-wafer-covering rapid thermal annealing (SWC-RTA) at 800°C for 15–60 s in N₂ ambient. After annealing, the substrate cooling duration down to 100°C was 14 min. The C'O (0.7 nm) layer was merged with HfON and Si atoms that diffused into the HfON layer from the Si substrate during plasma oxidation and PDA. The concentrations of Si and N atoms in the HfSiON layer were approximately 10 and 20%, respectively. After gate electrode patterning by lithography, the selective etching of HfN layer at room temperature was carried out utilizing DHF (1%) and a mixed solution (HF:H₂O₂:H₂O = 1:2:40) [11]. Finally, Al electrodes were evaporated on the back surface of p-Si(100) substrates. The fabricated MIS diodes were characterized by capacitance-voltage (C-V) and current-voltage (J-V) methods. The EOT was evaluated using EPOQUE with quantum mechanical correction [12]. Atomic force microscopy (AFM) was also carried out to characterize a roughness at the HfN/HfSiON interface.

3 Results and discussion

Figures 1(a) and 1(b) show the etching duration for removing 40 nm-thick HfN, HfSiON, and HfN/HfSiON gate stacks formed on p-Si(100) by DHF (1%) and mixed solution (HF:H₂O₂:H₂O = 1:2:40), respectively. The end point of the etching was determined by hydrophobicity of Si surfaces. From Figs. 1(a) and 1(b), it was confirmed that etching duration of mixed solution was approximately 10 times shorter than that of DHF (1%), that is, etching rate of mixed solution was higher. The calculated etching rate of HfN was 0.23 nm/s for DHF (1%) and 2.9 nm/s for the mixed solution. In addition, etching duration of HfN/HfSiON gate stacks was equal to the sum of that of HfN and that of HfSiON for both etchants. Therefore, it can be said that selective etching of HfN in HfN/HfSiON gate stack is possible. Furthermore, the etching time of HfSiON became longer after PDA. Etching rate ratios of HfN to HfSiON ($v_{\text{HfN}}/v_{\text{HfSiON}}$) with PDA were 18.5 and 65 for DHF (1%) and the mixed solution, respectively. From above-mentioned results, the mixed solution (HF:H₂O₂:H₂O = 1:2:40) was suitable for selective etching of HfN metal gate in the HfN/HfSiON gate stack structure with PDA.

Fig. 1. Etching duration for removing HfN, HfSiON, and HfN/HfSiON by (a) DHF and (b) mixed solution.

Next, an annealing duration dependence of HfN/HfSiON/p-Si(100) was studied to evaluate an interdiffusion at interfaces during the annealing process. Figure 2(a) shows annealing duration dependences of RMS surface roughness obtained by etching of HfN in HfN/HfSiON gate stacks, which were annealed at 800°C for 15–60 s, by mixed solution. The related AFM images of HfSiON surfaces are also shown that the etching duration was 24 s for annealing duration of 60 and 15 s, respectively. From Fig. 2(a), the etching of HfN was preceded with RMS roughness of 0.6 nm. It was found that RMS surface roughness of HfSiON in HfN/HfSiON gate stacks annealed at 800°C for 60 s was increased at the etching duration of 24 s. In addition, relatively flat surface was observed for the sample after 800°C/15 s PDA, while some projections were locally observed at the interface in case of a longer PDA duration. These results suggested that projections on the HfSiON surface were formed by local diffusion of Si atoms to HfN layer when the PDA duration was longer, as illustrated in Fig. 2(b).

Finally, an annealing duration dependence of electrical characteristics was investigated. C-V and J-V characteristics of HfN/HfSiON/p-Si(100) gate stack structures annealed at 800°C for 15–60 s were shown in Figs. 3(a) and 3(b), respectively. From Fig. 3(a), it was confirmed that C-V characteristics with a negligible hysteresis and without stretch of C-V curve were obtained after PDA. In addition, the EOT was reduced to 0.56 nm in case of 800°C/15 s PDA, compared with the EOT of 0.6 nm obtained by 800°C/60 s PDA. Therefore, the thickness of IL was increased by O atoms diffusion caused by longer duration of PDA. Furthermore, from Fig. 3(b), the leakage current at $V_{FB}-1$ V was decreased from 8.7 to 1.3 A/cm² which is compatible value for HfSiON thin film by shortening an annealing duration from 60 to 15 s [13]. It can be said that suppression of local projection formation by shortening annealing duration resulted in the improvement of interface properties.

4 Conclusion

The selective etching of HfN gate electrode in HfN/HfSiON gate stack structures was investigated. In comparison of DHF (1%) and mixed solution

Fig. 2. (a) Annealing duration dependence of RMS roughness. AFM images of HfN/HfSiON interface are shown with annealing duration of 60 and 15 s. (b) Schematic for a reaction model at the HfN/HfSiON interface.

Fig. 3. Annealing duration dependences of (a) C-V characteristics and (b) J-V characteristics.

(HF:H₂O₂:H₂O = 1:2:40) for the etching rate ratio of HfN to HfSiON, it was found that 65 times etching selectivity of HfN to HfSiON was realized by the mixed solution, which was 3 times higher than the selectivity of DHF (1%). Furthermore, it was confirmed that HfN/HfSiON/p-Si(100) gate stack structures would be formed by in-situ ECR plasma process using the selective etching technology. After selective etching of HfN in HfN/HfSiON

gate stacks, it was found that a reaction at the interface was suppressed by shortening the 800°C PDA duration from 60 to 15 s. In addition, the EOT was thinned from 0.6 to 0.56 nm and the leakage current at $V_{FB}-1$ V was decreased from 8.7 to 1.3 A/cm².

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