Time-distributed procedure for fast estimation of effective number of bits during ADC Design

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Abstract: This work proposes and analyzes an intuitive time-distributed procedure for estimating the effective number of bits (ENOB) of ADCs during the design phase. Two derived numbers, the ENOB lower-bound and the ENOB upper-bound, signal to a designer whether the design has satisfied the desired quality, or either further circuit improvement or a more accurate time-distributed procedure is necessary. The result enables designers to employ the procedure to almost linearly reduce the ENOB simulation waiting time with a controllable loss of accuracy. Two successive approximation register (SAR) ADC designs demonstrate the effectiveness of the procedure, one of which has been manufactured.

Keywords: effective number of bits, analog-to-digital converter, successive approximation register ADC

Classification: Integrated circuits

References

1 Introduction

Due to the close relation with the signal-to-noise ratio [1], the ENOB is a critical parameter of an ADC, especially in communication applications. Numerous studies have discussed fast testing methods for ENOB [2]. However, few have examined the fast estimation of ENOB during the design phase, which is the focus of this article. The former approach seeks to minimize total testing time while the latter seeks to minimize the simulation waiting time. As observed in many tape-out review meetings of the National Chip Implementation Center in Taiwan, a long simulation waiting time troubles many designers focusing on high-resolution SAR ADC, especially with calibration.

A SAR ADC mainly comprises a single comparator, a capacitor array, and a digital control block. Due to its simple analog circuit and its digital circuit easily benefiting from process improvements, a SAR ADC is a low-power architecture that has recently received widespread attention due to trends in mobile devices [3, 4, 5]. However, a high-resolution SAR ADC ENOB simulation is time consuming because its clock rate is not only proportional to its sampling rate, but also proportional to its bit resolution. Another reason is that the number of used capacitors doubles with the addition of one bit of extra resolution.

This work proposes a time-distributed procedure, which distributes the total simulation time to several sections before distributing each section to an available computer for simulation. Finally, the results are combined to calculate the ENOB. Regarding waiting time, the time-distributed procedure speeds up the ENOB simulation according to the number of distributed sections. This work contributes to the accuracy analysis, derives an ENOB lower-bound, an ENOB upper-bound, and the result enables the adoption of this simple method to reduce simulation waiting time with confidence.

In the end, this work provides two SAR ADC designs as examples: a single-ended design and a differential design, the latter of which has been manufactured.

2 Why time distribution is possible

An ADC converts an analog signal to a digital value. An ADC can ideally sample several sections of time separately without affecting the combined digital values. However, a practical ADC simulator behaves differently because a second-section simulator may, for example, have a different set of capacitor/inductor initial conditions compared to the corresponding conditions of a long single-section simulator. Due to the different initial conditions, a damping situation theoretically occurs at the junctions of the combined simulation. However, with an ADC of reasonable quality, such a difference should be small, or even negligible. Furthermore, a designer can extend each section a few sampling cycles backward to make the combination even smoother,
## 3 Estimated ENOB accuracy analysis

An ENOB equation can be rewritten from Chapter 9 of [1] as:

\[
ENOB = D_0 - \log_2 \left( \sqrt{\frac{1}{M} \sum_{n=1}^{M} (x[n] - x'[n])^2} \right)
\]

(1)

where \( M \) is the number of samples in the record, \( x[n] \) is the sample data set, \( x'[n] \) is the data set of the best-fit sine wave, and \( D_0 \) is a constant.

The ENOB simulation is assumed to be distributed to the \( k \) sections evenly and the combined data results to \( ENOB_k \). The corresponding sample data set is \( x_k[n] \), and the error is \( e_k[n] \), that is, \( x_k[n] = e_k[n] + x[n] \). Since the added error is assumed to be small, the study assumes that the data set \( x'[n] \) of the best-fit sine wave is unchanged. Thus, Eq. (2) is true, as demonstrated below:

\[
ENOB_k = D_0 - \log_2 \left( \sqrt{\frac{1}{M} \sum_{n=1}^{M} \left\{(x[n] - x'[n])^2 + e_k[n]^2 + 2(x[n] - x'[n])e_k[n]\right\}} \right)
\]

(2)

To simplify the derivation, this article assumes that each additional section has only one error term, the largest of which is \( \max(e_k[n]) \), resulting in Eq. (3).

\[
ENOB_k \geq D_0 - \log_2 \left( \sqrt{\frac{1}{M} \sum_{n=1}^{M} (x[n] - x'[n])^2 + \max(e_k[n])^2 + \sum_{n=1}^{M} (x[n] - x'[n])^2} \right)
\]

(3)

With a reasonable quality of ADC, this article further assumes that the different multisection combinations do not change the largest value of \( |x_k[n] - x'[n]| \); hence, \( \max(|x_k[n] - x'[n]|) = \max(|x[n] - x'[n]|) \) for each \( k \). This assumption is true as the study assumes the multisection combinations create relatively small perturbations. Consequently, Eq. (4) is true, as demonstrated below:

\[
ENOB_k \geq D_0 - \log_2 \left( \sqrt{\frac{1}{M} \left\{(k-1)\max(e_k[n])^2 + 2\max(|x[n] - x'[n]|)\max(e_k[n]) + \sum_{n=1}^{M} (x[n] - x'[n])^2\right\}} \right)
\]

(4)

Eq. (4) can be simplified to Eq. (5), as follows:

\[
ENOB_k \geq D_0 - \log_2 \left( \sqrt{\frac{1}{M} \sum_{n=1}^{M} (x[n] - x'[n])^2} \right) (1 + \varepsilon)
\]

(5)

where \( \varepsilon = \frac{(k - 1)\max(e_k[n])^2 + 2\max(|x_k[n] - x'[n]|)\max(e_k[n])}{\sum_{n=1}^{M} (x[n] - x'[n])^2} \).
Similarly, (6) is true, as shown below.

$$ENOB_k \leq ENOB - \log_2 \sqrt{(1 - \varepsilon)}$$

(6)

Furthermore, the study assumes that the multisection-induced error is negligible compared to the total error in the two denominators of Eq. (7). This assumption is to facilitate the development of lower-bound and upper-bound for ENOB later in Eq. (8) and Eq. (9) only. As long as the discrepancies between with and without the assumption are small, the assumption is reasonable. A detailed discussion is omitted here due to space limitation.

$$\varepsilon = \frac{(k - 1) \max(e_k[n]^2) + 2 \max(|x_k[n] - x'[n]|) \max(|e_k[n]|)}{\sum_{n=1}^{M} (x[n] - x'[n])^2}$$

$$\simeq \frac{(k - 1) \max(e_k[n]^2) + 2 \max(|x_k[n] - x'[n]|) \max(|e_k[n]|)}{\sum_{n=1}^{M} (x_k[n] - x'[n])^2}$$

(7)

Thus, the values used for calculating $\varepsilon$ can be obtained when $ENOB_k$ is obtained except for $\max(|e_k[n]|)$, which can be estimated by setting several fixed input signals and observing how the output digital values react to the corresponding fixed values. After obtaining an $ENOB_k$ value, a designer can calculate a lower-bound and an upper-bound for ENOB, which are written as Eq. (8) and Eq. (9), derived from Eq. (5) and Eq. (6), respectively.

$$ENOB_{lb} = ENOB_k + \log_2 \sqrt{(1 - \varepsilon)}$$

(8)

$$ENOB_{ub} = ENOB_k + \log_2 \sqrt{(1 + \varepsilon)}$$

(9)

If the $ENOB_{lb}$ satisfies the desired ENOB, the design is sound. Otherwise, and if the $ENOB_{ub}$ is still unable to satisfy the desired ENOB, reducing the number of distributing sections will be ineffective, and the designer must improve the design.

4 Two design examples

This article demonstrates the proposed procedure with two 10-bit SAR ADC designs. The first design has a single-ended input with architecture similar to [3] and with 2,600 MOS and 8,600 RC. The second design has a differential input with architecture similar to [4]. The ENOB simulation of a single section of the single-ended design and the differential design require 14 and 42 hours, respectively, on a computer with a 3.33 GHz six-core CPU. Fig. 1 shows the speed-up of the proposed time-distributed procedure considering with/without an initial condition solution time compared with the speed-up of the increasing core-number.

4.1 The single-ended design

For this design, the sampling rate is 910 kHz, and the used input frequencies
Fig. 1. Distributed speeds and multi-core speed comparison

are 90 kHz and 405 kHz. The number of samples for each ENOB calculation is 1024. The error term \(\max(|e_k[n]|)\) is estimated according to the output digital value-settling situation of 20 fixed input values between the maximum and minimum possible input values. Most of the digital value sequences settle on the second value, with the first value one least significant bit (LSB) away from the settling value. Therefore, this work arbitrarily uses one LSB as the maximal distribution-induced error per additional distributed section, that is, \(\max(|e_k[n]|)=1\). Table I shows the input and derived values related to \(\text{ENOB}_k\), \(\text{ENOB}_{lb}\), and \(\text{ENOB}_{ub}\) with \(k=1, 2, 3, 4, 5, 6\) when input frequency is 90 kHz.

Since designers may be concerned with the largeness of the discrepancy between \(\text{ENOB}_k\), \(\text{ENOB}_{lb}\), and \(\text{ENOB}_{ub}\), Fig. 2 shows the relationships between \(\text{ENOB}_k\), \(\text{ENOB}_{lb}\), \(\text{ENOB}_{ub}\), and the distribution number \(k\). The largest discrepancy is 0.7%. The discrepancy is significantly less when the input frequency is 405 kHz because \(\sum_{n=1}^{M}(x_k[n] - x'[n])^2\) is larger, effectuating Eq. (7).

Table I. Values during the time-distributed procedure for the single-ended design

<table>
<thead>
<tr>
<th>(f_m=90,\text{kHz})</th>
<th>(k=1)</th>
<th>(k=2)</th>
<th>(k=3)</th>
<th>(k=4)</th>
<th>(k=5)</th>
<th>(k=6)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\max(</td>
<td>e_k[n]</td>
<td>)) (LSB)</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>(\max(</td>
<td>x_k[n]-x'[n]</td>
<td>)) (LSB)</td>
<td>1.68</td>
<td>1.67</td>
<td>1.68</td>
<td>1.68</td>
</tr>
<tr>
<td>(\sum_{n=1}^{M}(x_k[n]-x'[n])^2) (LSB²)</td>
<td>222</td>
<td>221</td>
<td>218</td>
<td>223</td>
<td>227</td>
<td>221</td>
</tr>
<tr>
<td>(\varepsilon)</td>
<td>0</td>
<td>0.020</td>
<td>0.040</td>
<td>0.059</td>
<td>0.077</td>
<td>0.098</td>
</tr>
</tbody>
</table>
4.2 The differential design

For the differential design, the sampling rate is 1 MHz, and the used input frequencies are 100.9 kHz and 450.7 kHz with 1024 samples. Similarly, the error term \(e_k[n]\) is estimated according to the output digital value-settling situation of 20 fixed input values between the maximum and minimum of possible input values. All digital output sequences settle on the first available values. Therefore, the work uses one LSB as the distribution-induced error per additional distributed section, that is, \(\max(|e_k[n]|)=1\). If zero LSB is used as \(\max(|e_k[n]|)\), each group of ENOB\(_k\), ENOB\(_lb\), and ENOB\(_ub\) is the same value.

Fig. 2. The relationships between ENOB\(_k\), ENOB\(_lb\), ENOB\(_ub\), and \(k\) for the single-ended design

Fig. 3. The relationships between ENOB\(_k\), ENOB\(_lb\), ENOB\(_ub\), and the distribution number \(k\) when input frequencies are 100.9 kHz and 450.7 kHz for the manufactured differential design
Fig. 3 shows the relationships between $\text{ENOB}_k$, $\text{ENOB}_{lb}$, $\text{ENOB}_{ub}$, and the distribution number $k$ for the differential design. The largest discrepancy is 0.4%. The design was manufactured with a 0.18 $\mu$m CMOS process, and the measured ENOBs are 8.4 and 8.6 for input frequencies of 100.9 kHz and 405.7 kHz, respectively.

5 Conclusion

This article proposed and analyzed an intuitive time distribution method with a controllable accuracy, indicated by two derived values, the ENOB lower-bound, and the ENOB upper-bound, to almost linearly reduce the ENOB simulation waiting time with the number of sections during the design phase. Two 10-bit SAR ADC design examples demonstrate the effectiveness of the procedure, one of which has been manufactured with satisfactory measurement results.

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