A 6-bit active digital phase shifter

Alireza Asoodeh^{a)} and Mojtaba Atarodi^{b)}

Electrical Engineering Department, Sharif University of Technology, Tehran, Iran

a) Alireza_asoodeh@yahoo.com

b) Atarodi@sharif.edu

Abstract: This paper presents the design of a 6-bit active digital phase shifter in 0.18- μm CMOS technology. The active phase shifter synthesizes the required phase using a phase interpolation process by adding quadrature phased input signals. It uses a new quadrature all-pass filter for quadrature signaling with a wide bandwidth and low phase error. The phase shifter has simulated RMS phase error of $<0.85^\circ$ at 2.4–5 GHz. The average voltage gain ranges from 1.7 dB at 2.4 GHz to -0.14 dB at 5 GHz. Input P1 dB is typically 1.3 ± 0.9 dBm at 3.5 GHz for overall phase states.

Keywords: active phase shifters, phased arrays, quadrature networks

Classification: Microwave and millimeter wave devices, circuits, and systems

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1 Introduction

Many communication and radar systems are based on phased array antennas

for achieving electronic beam control and fast beam scanning [1]. Phase shifters have been widely used in phased array antennas for electronic beam steering [2].

Traditionally electronic phase shifters have been developed with passive components. Although some of these passive approaches could provide true time delay, their physical dimensions make it impractical for integration with multiple arrays in a commercial (IC) process. Passive phase shifters also suffer from a large insertion loss, and therefore require an amplifier, typically more than two stages at K-band frequencies, to compensate for this loss [4].

Compared to passive phase shifters, active phase shifters can provide continuous phase shift or multi-bit operation with low loss or even gain [3]. In this work, we demonstrate a 6-bit CMOS active phase shifter.

2 Phase shifter architecture

Fig. 1 (a) shows the functional blocks of the active phase shifter. The underlying principle in this architecture is a phase synthesis by a signal interpolation which is done by adding two quadrature inputs. A quadrature all-pass filter (Q.A.F) splits the differential input signal into quadrature phased I/Q vector signals, which are added with proper amplitude weights and polarities in a differential adder. The adder is composed of two Gilbert-cell type signed-VGAs, giving an interpolated output signal with a synthetic phase of $\tan^{-1}(Q_o/I_o)$ and a each magnitude of $\sqrt{(I_o^2 + I_Q^2)}$. Differential amplitude weightings of input of the adder are accomplished through changing the gain of the VGAs differently. The I/Q DAC takes this role by controlling the bias current of each VGA.

3 Circuit design

3.1 Quadrature all-pass filter (Q.A.F)

In the phase synthesis, which is based on a phase interpolation method by adding two properly weighted quadrature vector signals, the accuracy of the output phase is dominated by the orthogonal precision of the I/Q seed vectors. Because of the dependence of the output phases on the amplitude weightings of I- and Q- input, the amplitude mismatch of this block can also affect the output RMS phase error. So, in order to gain a decent RMS phase error, both the amplitude mismatch ($A_{error} = |20 \times \log(V_{OI}/V_{OQ})|$) and the phase error ($\theta_{error} = 90 - (\theta_{OI} - \theta_{OQ})$) of this block must be zero or very small. To get zero amplitude mismatch, either an all-pass filter or a structure that makes $|V_{OI}| = |V_{OQ}|$ must be used. In [4, 5], a structure is proposed that follow the second option. This is shown in Fig. 1 (b). While this structure resolves the problem of the amplitude mismatch, it doesn't have a good phase error. It's so much that we cannot increase the phase shifter resolution to more than four bits (at the best, to five bits). But it should be said that if we want to increase the phase shifter resolution to more than four bits, the bandwidth should be largely decreased [Fig. 1 (g)] to gain a reasonable

Fig. 1. (a) The building blocks of the active phase shifter, (b) The conventional Q.A.F structure, (c) & (d) All-pass filters, (e) The proposed Q.A.F structure, (f) A typical curve of the output phase difference of the proposed QAF. (g) Maximum phase error (θ_{error}) vs. bandwidth ratio.

RMS phase error¹ in the output. In this paper, a new structure has been proposed that removes this problem; this makes θ_{error} very close to 0° in a very large bandwidth. The proposed structure which is the combination of the structures of Fig. 1 (c) and (d), has been shown in Fig. 1 (e). In order to convert this structure [Fig. 1 (e)] to all-pass filter and therefore the removal of the amplitude mismatch, the condition below must be satisfied.

$$R^2 = \frac{L_1}{C_1} = \frac{L_2}{C_2} = \frac{L_3}{C_3} \quad (1)$$

If this condition is satisfied, the input impedance will also be independent of frequency. A typical curve of the output phase difference of this network

¹A reasonable RMS phase error usually is smaller than $0.5 \times \text{LSB}$. For example, in a 6-bit phase shifter, this value is $0.5 \times 5.625^\circ = 2.8125^\circ$

[Fig. 1 (e)] vs. frequency has been shown in Fig. 1 (f). The transfer function and phase- error from 90°-relationships of the proposed structure are given in (2) and (3), respectively.

$$\begin{bmatrix} V_{oI} \\ V_{oQ} \end{bmatrix} = V_{id} \times \begin{bmatrix} \frac{R-j\omega L_1}{R+j\omega L_1} \\ \frac{(R-j\omega L_2)(R-j\omega L_3)}{(R+j\omega L_2)(R+j\omega L_3)} \end{bmatrix} \quad (2)$$

$$\theta_{error} = 90^\circ - 2 \times \tan^{-1} \left(\frac{L_1 L_2 L_3 \omega^3 + (L_2 + L_3 - L_1) R^2 \omega}{R^3 + R(L_1 L_2 + L_1 L_3 - L_2 L_3) \omega^2} \right) [deg] \quad (3)$$

The phase error (θ_{error}) will be equal to zero if $\tan^{-1}(x) = 45^\circ$ or $x = 1$. Where:

$$x = \left(\frac{L_1 L_2 L_3 \omega^3 + (L_2 + L_3 - L_1) R^2 \omega}{R^3 + R(L_1 L_2 + L_1 L_3 - L_2 L_3) \omega^2} \right) \quad (4)$$

Eventually, the element values vs. w_0 , w_1 and w_2 are:

$$z^3 - \left(\frac{1}{w_0} + \frac{1}{w_1} + \frac{1}{w_2} \right) z^2 - \left(\frac{1}{w_0 w_2} + \frac{1}{w_1 w_2} + \frac{1}{w_0 w_1} \right) z + \frac{1}{w_0 w_1 w_2} = 0 \quad (5)$$

$$z_1 = RC_3 = \frac{L_3}{R}, \quad z_2 = RC_2 = \frac{L_2}{R}, \quad z_3 : \text{Negative} \quad (6)$$

$$RC_1 = \frac{L_1}{R} = \frac{RC_3 - \left(\frac{1}{w_0} + \frac{1}{w_1} + \frac{1}{w_2} \right) + \sqrt{\left(\frac{1}{w_0} + \frac{1}{w_1} + \frac{1}{w_2} - RC_3 \right)^2 + \frac{4}{w_0 w_1 w_2 RC_3}}}{2} \quad (7)$$

Where w_0 , w_1 and w_2 are frequencies in which θ_{error} will be equal to zero.

To reach the element values that allow $|\Delta\emptyset_1| = |\Delta\emptyset_2| = |\Delta\emptyset_3| = |\Delta\emptyset_4|$ [Fig. 1 (f)], some computer programs such as matlab are needed. But, the primary values of elements can be guessed by using (5), (6) and (7). To do this, we can use the following algorithm.

$$w_0 = w_{min}, \quad \{0.75w_{min} + 0.25w_{max}\} < w_1 < \{0.5w_{min} + 0.5w_{max}\}, \quad w_2 = w_{max}$$

Where w_{min} and w_{max} are minimum and maximum frequencies, respectively [Fig. 1 (f)]. Finally, the software optimizes the primary values of elements gained by the above-mentioned algorithm to allow $|\Delta\emptyset_1| = |\Delta\emptyset_2| = |\Delta\emptyset_3| = |\Delta\emptyset_4|$.

For example:

$$\begin{aligned} [w_{min}, w_{max}] &= [10 \text{ GHz}, 18 \text{ GHz}] \\ \rightarrow w_0 &= 10 \text{ GHz}, 12 \text{ GHz} < w_1 < 14 \text{ GHz}, w_2 = 18 \text{ GHz} \end{aligned}$$

If $w_1 = 13 \text{ GHz}$, the element values are:

Using algorithm above:

$$\frac{L_1}{R} = RC_1 = 1.2 \times 10^{-11}, \quad \frac{L_2}{R} = RC_2 = 3.13 \times 10^{-12}, \quad \frac{L_3}{R} = RC_3 = 4.6 \times 10^{-11}$$

After optimization:

$$\frac{L_1}{R} = RC_1 = 1.186 \times 10^{-11}, \quad \frac{L_2}{R} = RC_2 = 3.12 \times 10^{-12}, \quad \frac{L_3}{R} = RC_3 = 4.51 \times 10^{-11}$$

As depicted, the gained values through the above-mentioned algorithm and after optimization are very close to each other.

Fig. 1(g) shows maximum phase error (θ_{error}) vs. bandwidth ratio ($[1 : w_{max}/w_{min}]$) for both structures. The phase error curve of the proposed structure is gained the interpolation of some points. To calculate these points, relations (3, 5, 6 and 7) and the above-mentioned algorithm are used. The relationship of maximum phase error vs. bandwidth ratio for the conventional structure is given in (8) [4, 5]:

$$MAX.\theta_{error} = 90 - 2 \times \tan^{-1} \left(\frac{2 \times x^{0.5}}{1 + x} \right)^{0.5} [deg] \quad (8)$$

As shown in Fig. 1(g), the phase error (θ_{error}) of the proposed QAF is closer to 0° in a very large bandwidth. For example, in the bandwidth ratio equal to 3.6, the maximum phase error is 5.5° for the conventional structure, whereas it's only 0.8° for the proposed structure.

3.2 Analog differential adder

Fig. 2(a) exhibits the differential signed-adder, which adds the I- and Q-inputs from the Q.A.F in the current domain at the output node, synthesizing the required phase [4, 5]. The size (16/0.18) of the input transistors (M_1 – M_8) is optimized thorough SPECTRE simulations with respect to gain in the same stage and the phase response in the prior stage. The polarity of each I/Q input can be reversed by switching the tail current from one side to the other side, with switches S_I and S_Q .

The DC model of a $0.18\text{-}\mu\text{m}$ CMOS can be well approximated to conventional long channel quadratic I-V model under the low-level gate overdriving. Therefore, the gain settings of the I- and Q- path of the adder for 6-bit phases

Fig. 2. Analog differential adder, current source and I/Q DAC structures for bias current controls of the adder, (a) The differential signed adder, (b) current source, (c) I-DAC, (d) Q-DAC.

in this work are based on the long channel model for simplicity and better intuition. For instance, a 43 : 12 ratio between $I_{I,Bias}$ and $I_{Q,Bias}$ results in $\sqrt{43} : \sqrt{12}g_m$ ratio between I- and Q- path of the adder leading to an output phase of $\tan^{-1}(\sqrt{12}/\sqrt{43}) \approx 27.85^\circ$, that it has only 0.28° error from 6-bit resolution.

3.3 I/Q DAC

Fig. 2 (c) and (d) show the I/Q DAC with typical size. For the 0° bit, by setting $S_{0,1,...,6} = \text{low}$, all the DAC element currents are directed toward I-path. For the 45° bit, a logic encoder sets $S_{0,1,4,5} = \text{low}$ and $S_{2,3,6} = \text{high}$ to make an equal current ratio between I- and Q- path in the DAC and the adder. It should be emphasized that the control logic for the switches and scaling of the current sources in the DAC are set such that for all 6-bit phase states, the load current in the adder is constant, i.e., $I_{I,Bias} + I_{Q,Bias} = \text{constant}$ for all phase bits. This results in a same gain response which is proportional to $\sqrt{(I_{I,Bias} + I_{Q,Bias})}$ for all phase states due to the square-root gain dependency on the bias current in CMOS. The tail bias current ($I_{I/Q,Bias}$) equation vs. the reference current can be written as:

$$I_{out(=I/Q,BIAS)} = I_{ref} \times \frac{\left(\frac{W}{L}\right)_{out} \times (1 + \lambda V_{DS\ out})}{\left(\frac{W}{L}\right)_{ref} \times (1 + \lambda V_{DS\ ref})} \quad (9)$$

Where $(W/L)_{ref}$, I_{ref} and $V_{DS\ ref}$ are the “aspect ratio”, the current and V_{DS} of M_{29} , respectively and λ is the channel-length modulation coefficient. $M_{s1,2}$ ($\dots M_{s7,8}$) have been used to allow $V_{DS\ out} = V_{DS\ ref}$. This work has been done to minimize tail bias current variations due to temperature and process variations. These transistors operate in the weak inversion region. In the weak inversion region, the simplified equation of the drain source current is given by $I_{ds} = I_{dso} \exp(v_{gs}/n \times v_{TH})$ with these conditions for v_{gs} and v_{ds} :

$$v_{gs} < V_T - nV_{TH}, \quad v_{ds} > V_{TH} \quad (10)$$

Where n is the slope factor, I_{dso} is the zero bias current, V_{TH} is the thermal voltage and V_T is the threshold voltage. If we assume that the transconductance parameter ($k = \mu_{cox}W/L$) and the V_T of M_{S1} are equal to those of M_{S2} , respectively, and $V_{ds,M_{S1}}$ satisfies saturation condition given by (10), M_{S1} will operate in the weak inversion region. Therefore $I_{ds,M_{S1}} = I_{dso}$ and M_{S2} also operate in the weak inversion region. Therefore $I_{ds,M_{S2}} = I_{dso}$. As a result, we obtain the following equation which represent the imaginary short between the input and output terminal. $V_{gs,M_{S2}} = V_s - V_g = 0$ [6]. Therefore, $I_{I,Bias}$ or $I_{Q,Bias}$ will be equal to the multiple of I_{ref} . To improve the current matching, the DAC has been designed with long channel CMOS ($L = 1\ \mu m$) and the switches have been also removed from current path [Fig. 2 (c), (d)].

4 Simulation results

The phase shifter is realized in $0.18\text{-}\mu m$ TSMC CMOS technology (IP6M). The Q.A.F provides less than 0.43° of quadrature phase error and below

Fig. 3. (a) I/Q phase/amplitude error of the Q.A.F, (b) 6-b phases referred to 0°-bit, (c) Simulated insertion gain of the phase shifter, (d) S_{11} of the phase shifter, (e) RMS phase error, (f) RMS gain error.

−34.5 dB of S_{11} (in differential 50 Ω reference) at 2.4–5 GHz range. The peak I/Q amplitude error of Q.A.F is less than 0.22 dB. Fig. 3(a) shows the simulated I/Q amplitude and phase error of Q.A.F.

Fig. 3(b) exhibits the simulated insertion phase with 6-bit digital input codes. Referenced to the 0° bit, the RMS phase error is less than 0.85° at 2.4–5 GHz. The insertion gain characteristics are shown in Fig. 3(c) and the RMS phase errors and gain errors versus frequency are presented in Fig. 3(e), (f), respectively. In the SPECTRE simulations, the phase shifter shows −0.14 ~ 1.7 dB of average voltage gain at 2.4–5 GHz. The peak gain variance is less than 0.65 dB for all 6-bit phase states. The simulated S_{11} is below −34 dB in the differential 50 Ω reference at 2.4–5 GHz. The phase shifter exhibits typically 1.3 dBm of input P1 dB at 3.5 GHz with ± 0.9 dBm variations for overall phase states. The phase shifter consumes a 2.5 mA current from a 1.8 V power supply.

5 Conclusion

In this paper, a CMOS 6-bit active digital phase shifter simulated in 0.18- μm has been presented. The fundamental operation of the active phase shifter is to interpolate the phases of the quadrature input signals by adding two

I/Q inputs. The proposed differential quadrature networks are developed to minimize the phase error and to increase the operating bandwidth with excellent signal precision in the phase shifter. To the best of the authors' knowledge, this Q.A.F structure has the smallest phase error in the wide bandwidth.