A high efficiency DC-DC Converter using a new in-package structure of Bonding-Wire inductor

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Abstract: In this paper, a new in-package high efficiency voltage down converter (VDC) is presented. Usually, quality factor of inductors is the main problem for generating high efficiency DC-DC Converters. In order to mitigate this problem, Bonding Wires with a new form are exploited in which four mutual inductions of bonding wire are used to increase the total inductance. This technique provides a high quality and low space in-package inductor with negligible parasitic elements. The peak efficiency for the proposed circuit at 50 MHz switching frequency is around 86\% with 150 mA loading current.

Keywords: in-package inductor, Voltage Down Converter (VDC), Bonding Wire, mutual inductance

Classification: Integrated circuits

References


1 Introduction

Recently Portable battery-operated devices are more popular with the main demands of small size, light weight, and long battery run-time. The batteries are the main portion of these portable devices. In addition, in the integrated systems, multiple power supplies have become common due to the coexistence of low-power digital circuits and analog/RF circuits. As a result, enhancing the efficiency of power supply is very important to extend the battery run-time.

Due to the increase of conversion ratio between the battery voltage and operating voltage, and increasing of current consumption, conversion efficiency has come to attract widespread attentions. Therefore multiple-VDD implementation is required in low power and high performance systems [1].

Voltage regulators, Switched capacitor converters and Buck converters are well known circuits for DC-DC converting. Voltage regulators have low efficiency and are suitable for low current loads. Switched capacitor converters need large capacitors and have poor performance in high demand current loads. A buck converter requires large passive elements of inductor and capacitor (LC) for an output filter but it shows higher power efficiency than other converters. The efficiency of on-chip buck converters is reduced by low quality factor of inductors. In spite of, numerous methods which investigate to access high quality factor inductors; Inherent characteristics of monolithic inductors prevent to develop the quality factor [2]. A high inductance with a high quality factor is presented by an initiative method of Bonding Wire connections. Using this technique, small size and high efficiency in-package DC-DC converters can be designed.

2 Proposed Bonding wire inductor

Proposed structure to make inductors is based on Bonding Wires (BW). Different methods are used in packaging, such as Ball Grid Array (BGA), Chip on Board (COB) and Flip-chip [3]. Despite the emergence of new packaging and interconnect technologies, bonding wire remains the dominant conventional low cost, high reliability and high manufacturability chip connection technology.

Due to large inductance caused by a typically thin wire diameter and small capacitance between the wire and the ground plane, sometimes BWs are used in RF circuits for generating low inductance monolithic inductors [4].

Our idea to solve this problem, resulted from magnetic relationships, is using of corner BWs with parallelizing them to achieve more inductance. The same direction currents fortify each other while the opposite direction ones deteriorate each other and perpendicular currents do not affect themselves. By utilizing the help of positive mutual inductance and corner wires we achieve a reasonable inductance.

Thin and long wires exhibit more inductance and also more resistance than thick and short wires. Self Inductance, mutual inductance and resis-
The inductance calculations of bonding wires are all given by the Eq. (1) and Eq. (2) [5]:

\[
L(\mu H) = 0.002l \left( \ln \left[ \frac{2l}{r} \right] - 0.75 \right) \quad \& \quad R = \frac{\rho l}{A}
\]  

\[
M(\mu H) = 0.002l \left( \ln \ln \left[ 1 + \sqrt{1 + \frac{l^2}{d^2}} \right] - \sqrt{1 + \frac{d^2}{l^2} + \frac{d}{l}} \right)
\]

Where \(l\) and \(r\), are the length and radius of wire, \(d\) represents the distance of two parallel wires, \(\rho\) shows the permeability and \(A\) is the cross section area of a wire.

Proposed topology is outlined in Fig. 1 (a). Four BWs that connected with two board-wires are used to realize in-package high quality inductor; we tried to find a way without any changing the structure of normally bonding wire connection, which utilizes the new structure to satisfy our requirements. The wires (bw1, bw2), (bw3, bw4) are planned to be vertical together to mitigate the negative mutual inductance which has harm effect due to their opposite current direction. However bw1 and bw2 are proposed to be parallel to fortify themselves because they have the same current direction. bw3 and bw4 have the same position. Similar plan was employed on the printed circuit board; w1 and w2 help each other to increase inductance.

**Fig. 1.** (a) Proposed interconnect bonding wires. (b) Simulated planar square inductor. (c) Wires Equivalent bonding wire inductor.
Proposed equivalent circuit is depicted and the parasite elements are also calculated with MATLAB. The most important formulas for calculating the inductance, mutual inductance and resistance were shown in Eq. (1), Eq. (2) and Eq. (3). Typical wire diameters used in the packaging are 25–50 μm that the thick wires are exploited to achieve low resistant connections. Two board wires are employed to connect four pin of IC as illustrated in Fig. 1 (a). Equivalent manufactured bonding wire inductor is depicted in Fig. 1 (c).

3 Control circuit design

With the use of smaller passive components, the resonant frequency of the output filter $f = \frac{1}{\sqrt{LC}}$ increases. Usually, in monolithic buck converters switching frequency is above 200 MHz that dominates transistor switching losses instead of inductor losses. To maintain the conditions of continuous mode operation under worst case condition, with respect to $V = L(\Delta I/\Delta T)$ below equation must be satisfied:

$$V = V_{DD} - V_{out} \quad \& \quad \Delta I = 2 \times I_{out(min)} \quad \& \quad \Delta T = \left( \frac{V}{V_{DD}} \right) \times \frac{1}{f} \quad (3)$$

Where $V$ is the voltage across the inductor, $\Delta I$ is the peak ripple current and $\Delta T$ is the time duration when the current is ramping up in the inductor, or the on-time of the PWM.

4 Simulation results

The quality factor that the inductance exhibits can be calculated by below formula.

$$Q = 2\pi \frac{\text{Peak magnetic energy} - \text{peak electric energy}}{\text{energy loss in one oscillation cycle}} = \frac{L\omega}{R} \quad (4)$$

where $R$ is series resistance of the inductor. With calculating parameters for proposed BW inductor, $Q$ is achieved about 8.0 which is considerable to the on-chip and in-package inductors.

For comparison we will show the differences between a planar inductor that simulated with ASITIC software and BW inductor parameters. Variety of planar inductors were designed and experienced to reach a high efficiency and reasonable VDC. One of them which its equivalent inductance equals with BW is introduced.

Fig. 1 (b) illustrates a planar square inductor. Metal layer is four, the metal widths are 30 μm and the occupied are $600 \times 600 \mu m^2$. The simulation results show 16 nH inductor with 0.3 quality factor. When the proposed planar inductor was substituted instead BW inductor in the circuit, the efficiency was only 55%.

Low power is dissipated in bonding wire inductor due to the negligible parasitic components of this type of inductors and main power is dissipated in MOSFETs. The proposed DC-DC converter with bonding wire inductor is implemented by TSMC 0.35 μm CMOS process and simulated in HSPICE.
It produces a stable output voltage with the range of 1.5 V to 2.5 V at the input voltage of 3.3 V. Fig. 2 (a) shows the efficiency of the proposed structure as a function of output current in 1.5 V and 2.5 V output voltages. As shown in the figure, the highest efficiency 86% is achieved at 150 mA loading current whereas the maximum current 500 mA can be delivered to the load.

The output voltage of the converter at 2.5 V and loading current 125 mA

Fig. 2. (a) Efficiency versus load current for various output voltages. (b) Output voltage of the converter at 2.5 V and 150 mA loading current.
is shown in Fig. 2 (b). Voltage ripple at 50 MHz switching frequency is 10 mV when 100 nF filter capacitance is utilized.

Establishing BW inductor helps us to improve the quality factor and efficiency in addition of area saving. Less switching frequency and voltage ripple with higher efficiency compare to the other on-chip or in-package DC-DC converters are noticeable. In addition, occupying small size in-package (0.05 mm²) is an important factor for this type of converters. Standard 0.35 μm CMOS process and the small size of converter prepared inexpensive in-package DC-DC converter. Realization about 16 nH bonding wire inductor that is achieved with establishing positive mutual inductance and suppressing negative mutual inductance, help us to receive well results.

The step response demonstrates the performance of the high bandwidth control loop. For a 50% load step from 0 to 250 mA, the converter achieves about 2% output voltage droop which is unprecedented sample. Highest voltage ripple from 0 to 250 mA is 11 mv that couldn’t get simply with traditional on-chip or in-package DC-DC converters.

For simplifying comparison, main performance parameters of this work with other on-chip or in-package buck converters are mentioned in Table I.

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<th>Table 1. Performance summery and comparison with other works.</th>
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<td>Process (nm)</td>
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<td>Inductor area</td>
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<td>Inductor per phase</td>
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<td>Peak efficiency</td>
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5 Conclusions

An in-package high efficiency DC-DC Buck converter with a low output voltage ripple is presented. 0.35 μm CMOS process is implemented for simulating proposed circuit. Realization of filter inductor with an initiating connecting method of bonding wires causes to achieve a high quality factor inductor with
negligible parasitic components in addition to occupying small area. Utilizing 50 MHz switching frequency with 100 nF filter capacitance cause to achieve 86% peak efficiency at 150 mA loading current with a 10 mv voltage ripple.