Energy and area-efficient tri-level switching procedure based on half of the reference voltage for SAR ADC

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Abstract: An energy-efficient tri-level switching scheme based on half of the reference voltage (V_{ref}) is proposed for the successive approximation register (SAR) analogue-to-digital converter (ADC). With respect to the set-and-down switching scheme, the common-mode voltage variation at the input of the comparator reduces. By using $V_{ref}/2$, the switching energy and the capacitor area are reduced. The proposed scheme achieves 97.26% less switching energy with one forth of the capacitor area as compared to the conventional architecture.

Keywords: SAR ADC, Reference voltage, DAC, capacitor array, energy, common-mode voltage

Classification: Integrated circuits

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1 Introduction

SAR ADCs are widely becoming attractive in low-power moderate-resolution/moderate-speed applications [1]. In SAR ADC, the sources of power consumption are capacitor array, comparator, SAR logic, and reference buffer.

Capacitor array and comparator dominate the power dissipation in SAR converter [2]. Furthermore, the capacitor array occupies the most part of chip area. Recent switching schemes have been proposed to reduce the switching energy and/or unit capacitor numbers using three voltage levels such as V_{cm} -based [3] and [4]. V_{cm} -based switching saves 87% of the switching power for 10-bit resolution, and needs 2^{N-1} unit capacitance [3]. Tri-level switching method in [4] reduces the switching power by 96.89% and saves the 75% area with respect to the conventional switching. However, this method drives the capacitor array output to converge toward $-V_{in}$ or V_{in} instead of V_{cm} . Consequently, the resolution of the comparator decays at the end of the bit-cycling when the input for the comparator is lowered. Further, in [4], V_{cm} must be equal to $V_{ref}/2$ which makes comparator design more challenging. In this Letter, a new tri-level switching scheme is reported to reduce both power consumption and capacitor area considerably with respect to conventional switching by using V_{ref} , $V_{ref}/2$, and V_{gnd} as references in the capacitor array.

Fig. 1. Input sampling phase for 5-bit SAR ADC and three first MSBs extraction ($V_{ref}/2$ is shown by V_{ref-h})

2 Tri-level switching scheme based on $V_{ref}/2$

The proposed structure for a 5-bit SAR ADC is shown in Fig. 1. The capacitor array contains 2^{n-2} unit capacitors which is one fourth of the conventional SAR ADC. The input is sampled on the top-plates of both capacitor arrays when the bottom plates of all capacitors are connected to $V_{ref}/2$. The first comparison does not consume any switching energy. After sign bit determi-

nation, the bottom plates of the capacitor array in one side are grounded and the second bit is decided. If the input is less than $V_{ref}/2$ and higher than $-V_{ref}/2$, the monotonic switching is employed to determine the rest of the bits using only $V_{ref}/2$. While the input is out of this range, the bottom plates of the capacitor array which stores the lower input voltage is switched to V_{ref} . In the latter, the switching of the array which uses $V_{ref}/2$ is the same as switching for signals smaller than $V_{ref}/2$. The switching of the array that employs V_{ref} is a little different, as shown in Fig. 2 (a).

In the proposed switching scheme, both capacitor array output voltages change simultaneously towards $V_{cm}-V_{ref}/4$ and V_{cm} according to sequences shown in Fig. 2(a) and Fig. 2(b), respectively. In contrary to [4], the input signal common-mode voltage does not need to be exactly equal to $V_{ref}/2$ which facilitates comparator design in lower supply voltages. Since the DAC outputs converge to V_{cm} or $V_{cm}-V_{ref}/4$, the problem caused by signal-dependent dynamic offset is relaxed.

Fig. 2. Switching sequence for determining forth bit for positive input (MSB=1): (a) $V_{ip}-V_{in} > V_{ref}/2$, (b) $0 < V_{ip}-V_{in} < V_{ref}/2$

The proposed switching method operates in a similar way as the tri-level technique [4] for determining first two MSBs. Both reduce the capacitor count by 75% and avoid the two first MSBs transition energy and settling time but the polarity of $V_{ref}/2$ voltage stored on the capacitor arrays is opposite. Accordingly, in the proposed method, for 2nd-MSB estimation, the bottom

plates of the capacitor array with the lower stored input are switched to V_{ref} . There is no charge redistribution and energy consuming for the capacitor array in determining of 2nd-MSB. The main difference of the proposed work with [4], is the switching sequence for the determinations of the remaining bits. The tri-level approach in [4] uses single-sided switching technique which makes the DAC common-mode voltage level signal-dependent. However, in the proposed method, both arrays switch during the conversion phase. In this way, the common-mode voltage of comparator is controlled. Since only one capacitor is switched at a time, the switching activity is the same as single-sided switching technique. The proposed scheme utilizes only $V_{ref}/2$ switching for resolving small input swings ($1V_{refP-P}$) which results in more energy efficiency compared with [4] counterpart for small signals.

3 Switching energy consumption

The behavioural simulation of a 10-bit SAR ADC based on the proposed scheme and recently published switching methods are compared in Fig. 3. Table I summarises the comparison of the switching energy, area and V_{cm} variation for different switching schemes. The proposed switching consumes 97.26% less energy and occupies 25% capacitor area compared to the conventional switching method. For half input swing ($1V_{refP-P}$), the proposed scheme consumes $14.61CV_{ref}^2$ average energy which is 31% more energy efficient with respect to single-sided switching in [4] in this input range. However, the energy efficiency degrades out of this range because of using V_{ref} in switching for full range signals.

Fig. 3. Switching energy against digital code

The partly asymmetric sequence of the switching after the 3rd-MSB estimation, equates to extra digital logic power consumption. On the other hand, input common-mode voltage variation is decreased, which reduces power con-

Table I. Average switching energy, energy and area saving ratio comparison for 10 bit SAR ADC

Scheme	Av. switching Energy CV_{ref}^2	Energy saving	Capacitor count	Converge voltage	No. of switches
Conventional [2]	1363.33	Reference	2^n	V_{cm}	$4N+10$
Monotonic [1]	255.5	81.26%	2^{n-1}	0	$4N$
Vcm-based [3]	170.16	87.52%	2^{n-1}	V_{cm}	$5N$
Single-sided [4]	42.41	96.89%	2^{n-2}	V_{in}	$6(N-1)$
Proposed	37.24	97.26%	2^{n-2}	V_{cm} $V_{cm}-V_{ref}/4$	$4N$

sumption and design effort of the comparator. Therefore, it can be concluded that digital power is traded off with the comparator power. However, the digital power further decreases with the technology advancement but comparator power is limited by noise and mismatch requirements. The digital control logic complexity is linearly related to the number of switches in SAR ADC. The previous tri-level switching methods like [3] use N more switches to utilize V_{cm} voltage level for a N -bit ADC. However, the proposed method needs $4N$ switches which is fewest among tri-level switching methods.

4 Conclusion

A three-level switching scheme is presented for SAR ADC. This switching scheme reduces switching energy by 97.26% with 75% area saving thanks to using $V_{ref}/2$ as a reference voltage. With half input signal swing, energy saving is more pronounced. Since the variation of the common-mode voltage is limited, the comparator design requirements are relaxed. The proposed switching scheme uses fewest switch and capacitor count among the published tri-level switching methods.