Answer to Comment on “High performance low-voltage QFG-based DVCC and a novel fully differential SC integrator based on it”

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References


1 Introduction

The following statements will answer to reported comments one by one:

I) First note is all right, that means the X terminal of DVCC in Fig. 1.(d) of [1] must be connected to common drain of M\(_5\) and M\(_6\). Also M\(_{11}\) and M\(_{21}\) transistors in first stage can be renamed to M\(_{1a}\) and M\(_{2a}\).

We great thank dear authors for noting these drawing mistakes.

II) Second note isn’t acceptable by us. We well know, as mentioned by Eq. (1) in [1] and experimental results from [11] in [1] and other published manuscripts, which well designed QFG circuits,
can work at frequencies from sub-Hertz to upper. At row 5 of Table I in [1] we mentioned “CM Input voltage range,” not “DC Input voltage range”! All of us know that common mode is said to all two identical signals, from DC to terahertz and above! Thus we don’t agree with dear authors in the statement “this is illogical and a significant error in the article”. But for Fig. 6 in [2] we agree with dear authors, in which “DC voltage transfer characteristics” should be replaced by “Quasi-DC voltage transfer characteristics”. However in Fig. 8 to Fig. 13 in [2], frequency range is from 1 Hertz to upper. Also in row 12 of Table I in [2], frequency range for $R_x$ is mentioned as from 1 Hz to upper.

III) Capacitors $C_2$ aren’t unnecessary as dear authors said: “… are connected to unnecessarily grounded capacitors ($C_2$)”. They construct the capacitor divider part of input stage.

IV) Improving dynamic range using QFG capacitive dividers is really an improvement; beside other methods for improving dynamic range (such as using complementary input stages). Overall gain of $A_v$ and $A_i$ are unity at the best conditions for CC’s!

V) Eq.’s (5) to (7) in [1] are correct. For an introduction and for simpler similar equations, interested users can refer to reference [4] in [1]. Beside, as mentioned in [1], assuming $I_{M15}$ equal to $I_{M16}$, $g_{mi} \gg g_{di}$, and circuit symmetry, $g_{m11}(g_{m1a})$ is equal to $g_{m1}$ and $g_{m21}(g_{m2a})$ is equal to $g_{m2}$; thus we don’t see $g_{m11}(g_{m1a})$ and $g_{m21}(g_{m2a})$ in Eq. (5), explicitly. Also our Eq. (6) written as $A_{i+} = \frac{i_{z+}}{i_x} = \frac{(g_{m7} + g_{m8})}{(g_{d7} + g_{d8})}$ is correct, not one written by Khateb et al. as: $A_{i+} = \frac{i_{z+}}{i_x} = \frac{(g_{m7} + g_{m8})}{(g_{d7} + g_{d8})}$. However, Eq. (6) must be rewritten as:

$$A_{i-} = \frac{i_{z-}}{i_x} \approx A_{i+} = \frac{i_{z+}}{i_x} = \frac{(g_{m7} + g_{m8})}{(g_{d7} + g_{d8})} / \left(\frac{g_{m5} + g_{m6}}{g_{d5} + g_{d6}}\right) \approx \frac{g_{m7} + g_{m8}}{g_{m5} + g_{m6}} \approx 1 \quad (6)$$

Whereas we wrote it in [1] as:

$$A_{i-} = \frac{i_{z-}}{i_x} \approx A_{i+} = \frac{i_{z+}}{i_x} = \frac{(g_{m7} + g_{m8})}{(g_{d7} + g_{d8})} / \left(\frac{g_{m5} + g_{m6}}{g_{d5} + g_{d6}}\right) \approx \frac{g_{m7} + g_{m8}}{g_{d7} + g_{d8}} \approx 1 \quad (6)$$

2 Conclusion

Although we thank dear authors Khateb et. al. a lot, for their investigating published paper [1], but as seen in above detailed answers, they can correct their mind about the manuscript.