Injection-locked fractional frequency multiplier with automatic reference pulse-selection technique

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Abstract: An injection-locked fractional frequency multiplier (IL-FFM) based on a ring VCO is proposed. The ILFFM can output signals whose output-frequency step equal quarter of an input reference frequency ($1/4 \times f_{\text{ref}}$), with low-phase-noise characteristics due to injection locking. To realize this fractional frequency multiplication, an injection pulse selection circuit is demonstrated, which can select the appropriate injection pulse trains as to the VCO output phases. The proposed circuit was fabricated in 65 nm CMOS process. When a 528-MHz ($f_{\text{ref}}$) reference signal was input, output frequencies of 4.5×, 4.75×, and 5×$f_{\text{ref}}$ were obtained with low phase noise. A 1-MHz-offset phase noise with injection was $-113$ dBc/Hz at the output frequency of 2.51 GHz ($=4.75 \times f_{\text{ref}}$).

Keywords: injection locking, frequency multiplier, ring VCO, CMOS

Classification: Microwave and millimeter wave devices, circuits, and systems

References


1 Introduction

Frequency multipliers and dividers with injection locking have been widely being used since they can easily achieve low-noise phase-locked clocks with simple circuit topologies. In the case of designing conventional injection-locked frequency multipliers (ILMFs), however, there is limitation that output frequencies ($f_{\text{out}}$) are only integral-multiplied by the reference frequency ($f_{\text{ref}}$), i.e. $f_{\text{out}} = f_{\text{ref}}, 2 \times f_{\text{ref}}, 3 \times f_{\text{ref}}, \ldots$. Therefore, the frequency resolution step becomes $f_{\text{ref}}$. To improve the resolution, $f_{\text{ref}}$ should be as low as possible, but lower $f_{\text{ref}}$ leads poor phase-noise characteristics.

As a solution, injection-locked fractional frequency multipliers have been already presented [1, 2, 3]. However, the proposed circuit in [1] just shows fractional frequency multiplication phenomena due to injection locking without explaining the mechanism. Circuits proposed in [2, 3] show automatic pulse-selection techniques with respect to the output frequencies, but they need complicated circuit topologies that only allow low-reference frequencies ($f_{\text{ref}}$). Compared with them, this paper proposes a simple pulse-selection technique to achieve a fractional frequency multiplication, which allows high-speed references to be input.

2 Proposed ILFFM

Fig. 1 (a) shows the proposed frequency multiplier, which consists of a multi-phase ring VCO, a bias-level shifter, an NAND-based pulse generator, and a pulse selector.

Fig. 1 (b) shows the proposed ring VCO. It consists of four-stage differential delay cells. Pseudo-differential delay cells and a bias-level shifter, proposed in [4], are employed to widen the frequency tuning range linearly. Injection pulses ($V_{\text{inj}}$) are generated from the input reference signal ($V_{\text{ref}}$) by the pulse generator. In the pulse selector, injection pulses are de-multiplexed and selected by using the VCO multi-phase outputs. The selected pulses are injected into two nMOS switches between the VCO differential nodes as shown in Fig. 1 (b). The switches would be on and short the differential nodes with pulse injection. Phase corrections are performed, and thus, phase noise can be reduced.

Fig. 1 (c) shows the proposed pulse selector topology. Four VCO output phases are used as a time-domain filter for the input pulses ($V_{\text{inj}}$). High-speed pseudo-nMOS latches are applied for selecting of high-speed reference clocks, minimizing the chip area, and achieving low power consumption [5].
input pulses are directly output when the latch clocks are high as shown in Figs. 1 (d) and (e). When the latch clocks are low, the pulse-selector output would be zero. In order to erase unwanted pulses, nMOS transistors at the output parts are employed to keep low-level output certainly. For example, pulses, which are injected slightly lead to VCO zero-crossing points between $V_{\text{out}0}$ and $V_{\text{out}180}$, are selected by using $V_{\text{out}90}$ and $V_{\text{out}270}$, simultaneously in Fig. 1 (d). With this topology, maximum four pulses trans can be obtained, which are de-multiplexed as to the VCO phases.
When the pulse period of $T_{\text{inj}} = 1.5 \times T_{01}$, pulses are de-multiplexed into two pulse trains ($V_{\text{inj}3}$ and $V_{\text{inj}4}$) whose period is $2 \times T_{\text{inj}}$ as shown in Fig. 1 (d). Also, they are de-multiplexed into four pulse trains ($V_{\text{inj}1}$, $V_{\text{inj}2}$, $V_{\text{inj}3}$, and $V_{\text{inj}4}$) whose period is $4 \times T_{\text{inj}}$ when $T_{\text{inj}} = 1.25 \times T_{02}$, as shown in Fig. 1 (e). In the same manner, input pulses are de-multiplexed into 1:1 when $T_{\text{inj}} = M \times T_{03}$ ($M = 1, 2, 3, \ldots$, $T_{03}$: VCO oscillation period). The de-multiplexed pulses are injected into the nMOS switches in Fig. 1 (b). As a consequence, appropriate pulse trains are automatically selected as to the output frequencies and the VCO output phases, and phase-locked and frequency-multiplied low-noise clocks can be achieved.

By using this pulse-selecting technique, the injection-locked output frequency range can be expressed as follows.

$$f_{\text{out}} = \frac{N}{4} \times f_{\text{inj}},$$

where $N$ is integer number of $N = (1, 2, 3, 4, \ldots)$ and $f_{\text{inj}}$ is the pulse frequency. The proposed technique can be applied in the case of an injection-locked frequency divider (ILFD) since the pulse-selecting topology has potential to operate at higher input frequencies than the output frequencies.

The upper limit of $N$ is determined with the power of superharmonics of the injected pulses. In other words, it would be determined from the relation between the pulse width and the ILFFM output period $T_0$. This is because the lock range of injection locking determined as follows, when $f_{\text{out}} = M \times f_{\text{inj}}$.

$$\omega_L = \frac{\omega_{\text{out}}}{2Q} \cdot \sqrt{\frac{P_{\text{injM}}}{P_{\text{osc}}}},$$

where $Q$ represents the open-loop quality factor of an oscillator (calculated by using the open-loop transfer function of the oscillator), $\omega_{\text{out}}$ is the output frequency of the oscillator under injection-locked condition, $P_{\text{injM}}$ is $M$th harmonic power of the injection pulse signal and $P_{\text{osc}}$ is the free-running output power of the oscillator [6]. Fig. 1 (f) shows narrower pulses are required to transfer the superharmonic power up to higher frequencies. However, the power ($P_{\text{injM}}$) of the selected pulses is degraded by the VCO jitter if the pulse width ($T_{\text{pwd}}$) is wide with respect to the ILFFM output rising/falling time as shown in Figs. 1 (d) and (e).

3 Measurement results

Fig. 2 (a) shows a chip micrograph of the proposed ILFFM. It was fabricated in 65 nm CMOS process. The core area is $30 \times 70 \mu m^2$, including the ring VCO, bias-level shifter, pulse generator, and pulse selector. The proposed circuit was measured with 1.2-V power supply voltage. External 528-MHz-square waves were used as reference signals, which are used in UWB applications requiring relatively higher-frequency references. The pulse generator produced short pulses of narrower than 80 ps from the input signals. When the control voltage was swept without injection locking, the VCO output frequencies were varied from 0.74 to 3.7 GH.
Fig. 2. (a) Chip micrograph, (b) frequency tuning range, frequency spectra at (c) 2.38 GHz, (e) 2.51 GHz, and (g) 2.64 GHz, phase noise characteristics at (d) 2.38 GHz, (f) 2.51 GHz, (h) 2.64 GHz.

Figs. 2 (b), (c), and (d) depict frequency spectra at the output frequencies of 2.38 GHz (= 4.5 × 528 MHz), 2.51 GHz (= 4.75 × 528 MHz) and 2.64 GHz (= 5 × 528 MHz), respectively. Measured reference spur levels were less than −34 dBc. In the conventional injection-locked oscillators, spurs would occur in steps of \( f_{\text{ref}} \) around the output carrier as shown in Fig. 2 (d). Since the proposed circuit realizes fractionally-integral frequency multiplication, spurs occurred in steps of \( f_{\text{ref}}/2 \) and \( f_{\text{ref}}/4 \) even if it used pulse-selecting technique. This is because that unwanted pulses were injected at unwanted places due
to VCO jitter, and VCO phase mismatches.

Figs. 2 (e), (f), and (g) show the phase-noise characteristics \((L(\Delta f))\) at the output frequencies of 2.38, 2.51, and 2.64 GHz, respectively. The phase noise characteristics at 1 MHz offset were \(-112\), \(-113\), and \(-114\) dBc/Hz, respectively, with pulse injection. Undesired spurs was observed at about 700-kHz-offset frequency, which were occurred due to the measurement environment.

Table I shows performance summary of the proposed frequency multiplier. The proposed circuit shows low power consumption and small area with acceptable phase noise.

### Table I. Performance summary.

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<tr>
<td><strong>CMOS technology</strong></td>
<td>65 nm</td>
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<tr>
<td><strong>Supply voltage ((V_{DD}))</strong></td>
<td>1.2 V</td>
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<tr>
<td><strong>VCO topology</strong></td>
<td>Differential ring VCO</td>
</tr>
<tr>
<td><strong>Tuning range</strong></td>
<td>0.74–3.7 GHz</td>
</tr>
<tr>
<td><strong>Reference frequency ((f_{ref}))</strong></td>
<td>528 MHz</td>
</tr>
<tr>
<td><strong>Output frequency ((f_{out}))</strong></td>
<td>2.38 GHz, 2.51 GHz, 2.64 GHz</td>
</tr>
<tr>
<td>(f_{out}/f_{ref})</td>
<td>4.5, 4.75, 5</td>
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<tr>
<td>(L(\Delta f)</td>
<td>_{\Delta f=1\text{MHz}})</td>
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<tr>
<td><strong>Power consumption</strong></td>
<td>8.9 mW, 9.4 mW, 9.9 mW</td>
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<tr>
<td><strong>Area</strong></td>
<td>0.0021 mm(^2)</td>
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### 4 Conclusion

The proposed fractional frequency multiplication technique is attractive as a method to improve the frequency resolution without degrading the phase noise. It only requires a multi-phase oscillator which has symmetrical properties, and the simple pulse selector.

The ILFFM was experimentally verified by using a 4-stage differential ring VCO, which was fabricated in 65 nm CMOS process. 1/2-, and 1/4-integral as well as an integral frequency multiplication can be realized with low phase noise characteristics. Consequently, the proposed technique could bring an impact in realizing a low-phase-noise high-resolution frequency multiplier.

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