

Advancement of superconductor digital electronics

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Abstract: Advancement of superconductor digital electronics, especially Rapid Single Flux Quantum (RSFQ) logic circuit is described. Ultra short pulse of a voltage generated across a Josephson junction and release from charging/discharging process for signal transmission in RSFQ circuits enable us to reduce power consumption and gate delay. The power-delay products (PDPs) of RSFQ integrated circuits (ICs) are 4 or 5 orders of magnitude smaller than those of semiconductor ICs. The fabrication process technology and the related designing technology have been advanced, and RSFQ ICs have been applied to software-defined radio receivers, superconductor detector array systems, and supercomputers. Recently, several kinds of energy-efficient single flux quantum circuit have been proposed to obtain further advantage to semiconductor devices. The PDPs of these circuits become at least 1 order smaller than those of conventional RSFQ circuits.

Keywords: single flux quantum, superconductor, energy efficiency, high-speed, power-delay product

Classification: Superconducting electronics

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1 Introduction

Superconductors have attractive natures as electronic devices. The macroscopic quantum effects, *i.e.* magnetic flux quantization in a superconducting loop and/or the Josephson effects [1] are the distinctive natures, and play the leading part in many applications such as magnetometers based on superconducting quantum interference devices (SQUIDs), voltage standards, and quantum computers.

The other attractive nature is extremely low surface resistances at high frequencies. This enables us to make resonators with high quality factors. Microwave bandpass filters based on superconducting resonators have been made of thin films of high-temperature superconducting materials. Trial introduction to commercial base stations of cellular phones has already begun in the United States.

In addition to the above-mentioned natures, strong non-linearity in resistance-temperature curves or two fluidity in superconductors are utilized in the operation of superconducting strip detectors such as transition edge sensors [2], microwave kinetic inductance detectors [3], superconducting nanowire single photon detectors [4]. These detectors attract increasing attention in nearly a decade because these are very sensitive to a variety of physical quantities.

Both the macroscopic quantum effects and low surface resistances are essential for the single flux quantum (SFQ) logic circuits [5, 6]. Integrated circuits (ICs) of the SFQ logic circuits have been demonstrated, and these SFQ-ICs have started to be applied to the radio receivers, superconductor detector array systems or computers because of their features of low power consumption, high-speed operation, *etc.* Most recently, a major trend in the SFQ circuits toward higher energy efficiency has been created in the United States [7, 8], and spread over the world [9, 10].

In this article, I review the development of the SFQ-IC-related technologies. I also describe the energy-efficient SFQ circuits.

2 Rapid single flux quantum circuits

There exists a macroscopic wave function describing the behavior of whole ensemble of superconducting electrons. Magnetic flux quantization is attributed to the quantum condition that the total phase change of the wave function around the superconducting loop must equal $2\pi n$ where n is any integer.

All the SFQ circuits use a quantized magnetic flux, *i.e.* an SFQ as an information carrier, though there are several types of SFQ circuits. In the original concept, the binary signal is obtained by recognizing the presence or absence of an SFQ in the loop [5]. In order to make an SFQ enter or leave the loop one at a time, superconducting weaklinks have to be inserted into the loop. A Josephson junction (JJ), a typical device exhibiting the Josephson effects, has a critical value of a superconducting current I_c named ‘the maximum Josephson current’ or ‘the critical current’. The I_c values used in SFQ circuits are about 4 orders of magnitude smaller than critical currents of superconducting thin films. In addition, I_c can be expressed by the periodic function of the phase difference of macroscopic wave functions between the two superconducting electrodes of a JJ. This means that JJs serve as weaklinks with a function of a doorway of an SFQ to the loop.

An impulse-shape voltage pulse called an SFQ pulse is generated when an SFQ crosses a JJ. Typical height and width of an SFQ pulse are 0.8 mV and 2.5 ps, respectively. As described later, the pulse width determines the clock period in SFQ circuits. Energy of 0.2 aJ is consumed at a JJ when an SFQ crosses the JJ with I_c of 0.1 mA. This energy consumption is 3 or 4 orders of magnitude smaller than that of semiconductor devices even for very high-speed operation.

Rapid Single Flux Quantum (RSFQ) circuit [6] is the most notable circuit among the SFQ circuits. In the original concept mentioned above, it is difficult to distinguish between the following two states; the state where a signal of the logical ‘0’ corresponding to the absence of an SFQ has already arrived at an RSFQ logic gate, and the other state where a signal of the logical ‘1’ has not arrived yet. To avoid this difficulty, clock signals are used for coding of RSFQ circuits. If an SFQ exists in a data path in time duration between adjacent two clock signals, the SFQ can be interpreted as the logical ‘1’. If there is no SFQ, it is the logical ‘0’.

Fig. 1 shows an equivalent circuit of a delay flip-flop (DFF), the basic element of RSFQ circuit. Each Josephson junction (JJ) has an external shunt resistor so as to satisfy the critical damping condition. As a result, the switching time becomes shortest, and stable operation of RSFQ circuit is guaranteed. In principle, the JJs are needed to be driven by current sources, because bias currents provided to the JJs are the driving forces for single flux quanta. However, a voltage source is employed in actual RSFQ circuits.

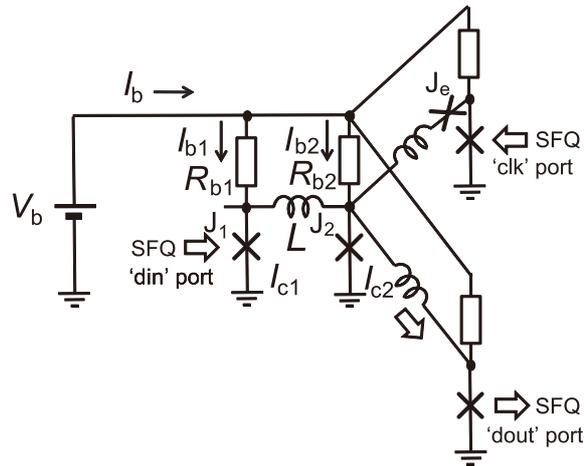


Fig. 1. Equivalent circuit of an RSFQ-DFF. X marks correspond to Josephson junctions.

Bias currents are provided through the bias resistors (for example, R_{b1} and R_{b2} in Fig. 1) connected to the voltage source as shown in Fig. 1. Typical supply voltage is 2.5 mV. This value is higher than $I_c R_s$ product, which is almost equal to the maximum voltage generated across the Josephson junction under the critical damping condition during the switching. Here, I_c is the critical current of a Josephson junction and R_s is the resistance value of the corresponding shunt resistor.

The operation of DFF is as follows: Bias currents of about 70% of the critical currents of grounded JJs are supplied. An SFQ serving as an input signal comes in at ‘din’ port. The sum of the circulating current of the SFQ and the bias current I_{b1} exceeds the critical current I_{c1} of J_1 . Then the J_1 is switched, and the SFQ goes to the storage loop consisting of J_1 , L , and J_2 . As mentioned before, an SFQ pulse is generated just when an SFQ crosses the junction. The pulse width τ_w is approximated by $\Phi_0/(I_c R_s)$, where Φ_0 is the magnetic flux quantum.

The LI_c product for the storage loop is set to be about Φ_0 , while the product of a non-storage loop is $0.5\Phi_0$. The circulating current accompanying a single Φ_0 in the storage loop is smaller than that in the non-storage loop. The sum of the circulating current and the bias current cannot exceed the critical current I_{c2} of J_2 , and an SFQ is stored.

The stored data are read out when an SFQ serving as a clock signal comes from ‘clk’ port to the storage loop. If an SFQ is stored, the total current flowing on J_2 exceeds I_{c2} . The two flux quanta are unified, and the SFQ goes to ‘dout’ port. If there is no SFQ in the storage loop, a clock SFQ escapes through J_e and no SFQ appears at ‘dout’ port.

Employing the coding of the RSFQ circuit, the maximum operating frequency is approximated by $1/(8\tau_w)$ in logic circuits. Typical $I_c R_s$ product is 0.8 mV for the critical current density J_c of 10 kA/cm², so that the frequency goes up to 50 GHz. Assuming the critical damping, $I_c R_s$ product is proportional to the square root of J_c . Thus, we can obtain the scaling law that the miniaturization leads to higher integration and higher operating frequency.

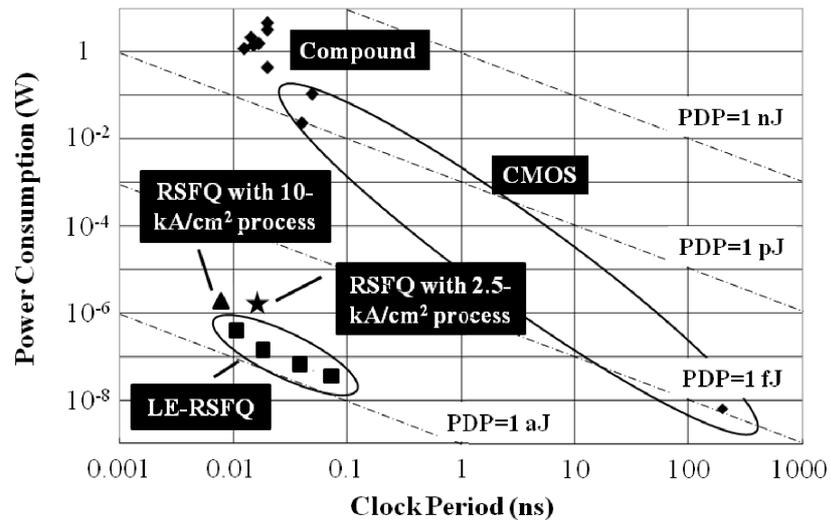


Fig. 2. Power consumption as a function of clock period for DFFs made with different technologies. LE-RSFQ circuit consumes less power, while clock period becomes long.

Fig. 2 shows clock period dependence of power consumption for DFFs made with different devices including semiconductors. The star and the triangle indicate the experimentally obtained data for RSFQ circuit fabricated with the ISTE (International Superconductivity Technology Center) 2.5-kA/cm² Nb IC technology [11] and that with the ISTE 10-kA/cm² technology [12], respectively. As indicated by the scaling law, the clock period for the DFF with the 10-kA/cm² technology becomes almost half compared to the DFF made with the 2.5-kA/cm² technology. The fastest RSFQ circuit is the digital frequency divider. That has been demonstrated up to 750 GHz by using 68 JJs with areas of 0.25 μm² [13].

The product of the power consumption and the clock period is called the power-delay product (PDP). The PDP is an important measure for the power efficiency in ICs. As seen in Fig. 2, complementary metal-oxide-semiconductor (CMOS) devices are better in the PDPs than in compound semiconductor devices, though the compound semiconductor devices can operate faster than CMOS devices. The PDPs of RSFQ circuits are 4 or 5 orders of magnitude smaller than for CMOS devices if clock period is smaller than 0.1 ns.

Passive transmission lines (PTLs) with microstrip or strip line structures are used for long interconnects, where a voltage pulse induced by an SFQ can travel at the speed of light. For using a PTL, a transmitter is placed between a logic gate and a PTL, and a receiver is placed between a PTL and a next gate. Fig. 3 shows operating margins in bias currents provided to a receiver as a function of lengths of PTLs. The PTLs under test had a microstrip line structure and was made on a single chip. Bias currents are normalized by a design value. Sufficiently wide margins exceeding ±20% are obtained below 50-mm-long PTLs, and a margin even for a 100-mm-

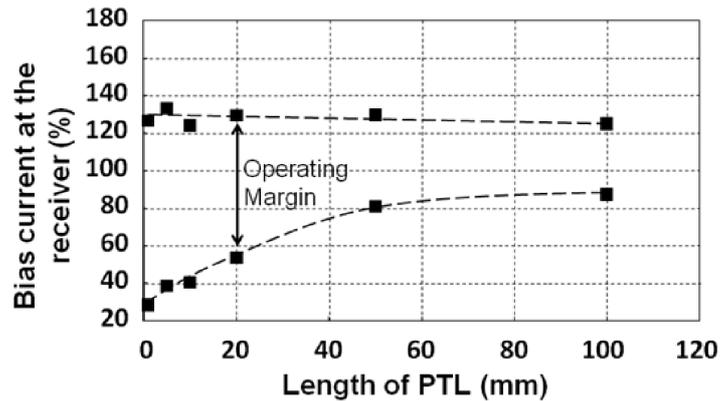


Fig. 3. Dependence of the operating margin on lengths of PTLs having the microstrip line structure based on the ISTEK 2.5-kA/cm² technology. Vertical axis shows bias currents provided to the receiver. The bias currents are normalized by the designed value.

long PTL is still within the acceptable range. This feature means that large band widths can be achieved not in on-chip (gate-to-gate) communication but also in off-chip (chip-to-chip) communication. In fact, 117-Gb/s chip-to-chip transmission has been demonstrated by using the ISTEK 10-kA/cm² Nb IC technology [14]. In addition, multicasting technique utilizing PTLs has already been developed [15] and used in many RSFQ circuits.

Power consumption at interconnects is an important issue. Needless to say, charging and discharging are needed for not only gate capacitances but also capacitances of interconnects in semiconductor field effect transistors including CMOS devices. Small gate capacitances have been achieved after downsizing, and values of gate capacitances become close to those of interconnect capacitances. As a result, delay times of interconnects determined by charging or discharging time of total capacitances often limit the operating frequencies. In addition, electric power required for charging is not negligible. When a 10-mm-long interconnect is driven at the data rate of 10 Gbit/s, a required power per 1 Gbit/s is about 10 mW/(Gbit/s) [16]. On the other hand, that with a 10-mm-long PTL is only 0.1 μ W/(Gbit/s) at present, which is 5 orders of magnitude smaller than the power for a semiconductor interconnect.

3 IC design technology

The delay times of interconnects both for clock lines and for data lines have to be controlled in RSFQ circuits, because binary signals are recognized based on the presence or absence of an SFQ corresponding to a data signal between consecutive clock signals. In particular, the control of delay times with a pico-second order is essential for operations under the concurrent-flow clocking, which has an advantage for any other clocking methods in operating speed. Note that delay time of a Josephson junction is sensitive to a bias current and that circuit parameters are spread in actual chips. These make the timing

control difficult in large-scale circuits.

To overcome this situation, introduction of the computer-aided-design (CAD) including an analog simulator and an optimizer is necessary. The CONNECT top-down design is described here as a typical CAD for the RSFQ circuits. The design is based on the CONNECT cell library [17]. Layouts of all the logic gates are designed in a rectangular shape. Input/output/clock ports are placed at the designated spots inside the rectangle. These layouts are called the logic cells. Josephson transmission lines (JTLs) and a PTL are used for interconnects. These are also designed in a rectangle and are registered in the library as the wiring cells.

Actual RSFQ circuits made with the ISTEK 2.5-kA/cm² technology are designed by putting logic cells and wiring cells. Circuit parameters of the logic cells are optimized so as to exclude the interference between adjacent cells and to operate with a large margin even under parameter spreads by using the circuit optimizer SCOPE [18]. The SCOPE can pick up the timing parameters such as setup-time, hold time, delay, *etc.* We examine the dependence of these parameters on the bias currents and register the bias-current-dependent timing parameters in the library. The timing design and its verification of the RSFQ circuits are carried out based on the registered timing parameters without doing analog simulation.

The initial CONNECT cell library was effective for circuits made up of about 5000 Josephson junctions. However, increased bias currents in larger-scale integrated circuits induce relatively large self magnetic fields, and reduce operating margins. To suppress self fields, all the logic cells registered in the present CONNECT cell library have superconducting shields for bias feed lines.

Logic cells based on the ISTEK 10-kA/cm² technology are also designed and registered in the library. Increased critical current density enables operations of 50–100 GHz and reduction of width of PTLs. Moreover, the 10-kA/cm² technology provides 9 Nb layers. The bottom Nb layer is used for distributing bias currents, and the top 4 Nb layers are almost the same as that of the 2.5-kA/cm² technology. Vertically stacked two strip line structures are formed by using the other 4 layers. Increased number of Nb layers leads to remarkable reduction in the circuit area, because PTLs can be placed below Josephson junctions.

Fig. 4(a) shows a microphotograph of a DFF cell made with the 2.5-kA/cm² technology. The dimension of a unit cell is 40 μm, and the DFF is designed in a 2-unit-long, 1-unit-wide rectangle. Fig. 4(b) indicates the DFF made with the 10-kA/cm² technology. The dimension of a unit cell is 30 μm. Pillars connected to the bottom layer are formed at each corner. Bias currents are provided to circuits through these pillars. Moats are formed around the pillars.

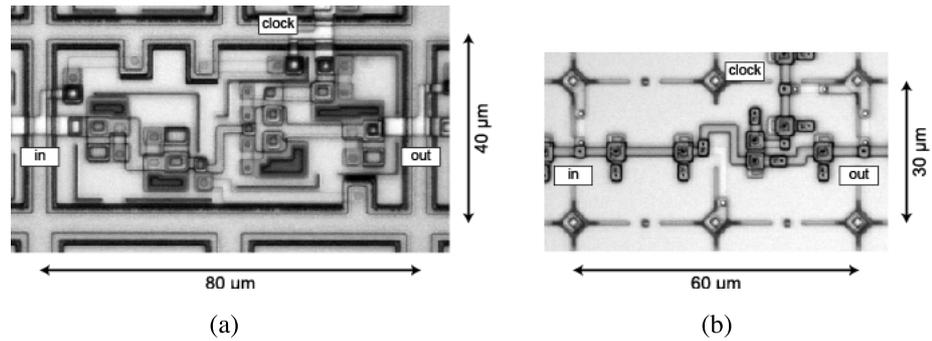


Fig. 4. Microphotograph of a DFF cell made with the ISTECH 2.5-kA/cm² technology (a), and that with the 10-kA/cm² technology (b). The DFFs are designed in a 2-unit-long, 1-unit-wide rectangle. The unit length is 40 μm for the 2.5-kA/cm² technology, and 30 μm for the 10-kA/cm² technology.

4 Applications of RSFQ circuits

The applications of RSFQ circuits can be classified into two major categories; the mixed signal and the information technology (IT). In the category of the mixed signal, analog signals are digitized at the front-end of RSFQ circuits. High-speed operation of RSFQ circuits enables high-frequency sampling, and utilizing flux quantization brings high precision in digitization. A software-defined-radio (SDR) receiver is a typical application in the mixed signal category [19, 20]. RSFQ-based SDR receivers can handle radio signals on single or multiple carrier waves directly. Almost all the components of a receiver including a down converter, a demodulator, and a channel selector are built with RSFQ logic circuits. These components are reconfigurable, and functions can be defined by software. RSFQ-based SDR receivers have extremely high flexibility to changes of modulation scheme, band widths, *etc.*

The key component of a receiver is a high resolution bandpass analog-to-digital converter (ADC). To achieve high resolution, the RSFQ-ADC has an oversampling delta- or delta-sigma-architecture, in which feedback of a flux quantum Φ_0 is involved. In addition, oversampling frequency is increased up to several tens of GHz. A good review for an RSFQ SDR application has been published in [21].

Another typical application in the category of the mixed signal is a superconductor detector array system. For last two decades, new superconductor detectors have been proposed and demonstrated [2, 3, 4]. Currently the development of superconductor detector systems places more focus on an array system in which multiple detectors are combined. Distinct advantage of RSFQ-based detector array systems to other RSFQ applications is ignorable penalty for cooling because low temperature circumstances are already used for a superconductor detector itself.

Configuration of a neutron diffraction system [22] based on MgB₂ thin film detectors [23] and an RSFQ signal processor is displayed in Fig. 5 as a typical example of a superconductor detector array system. All the sys-

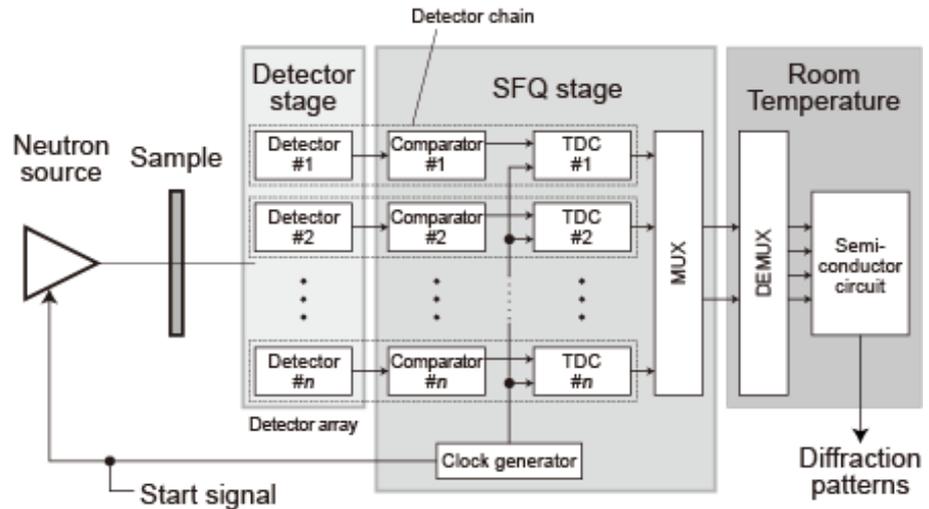


Fig. 5. Configuration of a neutron diffraction system based on MgB₂ thin film detectors and an RSFQ signal processor.

tems require more than 1000 detectors in the future. However, this leads to increased number of cables with which the detectors are connected to room-temperature electronics. Large heat inflow through these cables is unavoidable, so that the temperature of the detector stage becomes unstable in a conventional way. Thus, a low temperature multiplexing technique for the detector outputs is essential for reducing the number of the cables and for suppressing heat inflow. If detector outputs of interest are digitized, time-division multiplexing is achieved easily with RSFQ circuits because RSFQ circuits can operate at very high frequency.

In addition, intelligence is produced by using digital signal processing. For example, the key component for obtaining intelligence in the neutron diffraction system is RSFQ time-to-digital converters (TDCs). Time-of-flight of an incident neutron corresponding to energy of the neutron can be measured with an RSFQ TDC with high time resolution at low temperature.

The operation of the neutron diffraction system is as follows. A start signal generated at a room-temperature generator is provided repeatedly to the neutron source and all the TDCs. Triggered by each start signal, the source generates a flux of cold neutrons with various energies. These cold neutrons move to a detector array through a sample to be measured. Diffraction occurs in this process and diffraction pattern is obtained by counting the number of incident neutrons having a certain kinetic energy in each detector. Comparators based on a kind of SQUID judge whether a neutron comes to the corresponding detectors in every clock generated at the clock generator, and create an SFQ serving as a stop signal only in the case of neutron arrival. Each TDC measures a kinetic energy of a neutron by counting the SFQ pulses between the start signal and the stop signal. Introduction of a time domain multiplexer indicated as ‘MUX’ in Fig. 5 enables remarkable reduction in the number of cables between the SFQ stage and room-temperature electronics.

Fig. 6 shows a photograph of surrounding structures of the cold head in

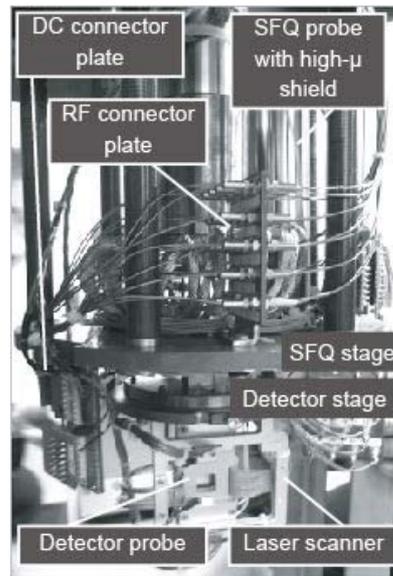


Fig. 6. Photograph of inside of a cryocooler used for a prototype of a neutron diffraction system. The RSFQ digital signal processor is mounted inside of a high- μ magnetic shield can on the SFQ stage (4 K). MgB_2 thin film detectors are placed on the detector stage (30 K). The structures seen in this figure are designed from many aspects such as noise, broad-band signal transmission, and thermal conduction.

our cryocooler used for the prototype of the neutron diffraction system. The SFQ stage is kept around 4 K, while the temperature of the detector stage is controlled to be just below the transition temperature of the MgB_2 thin film detectors. In the prototype, we have already demonstrated multiplexing of the TDC outputs for two detectors.

Applications in the IT category include supercomputers or data centers. Main circuits for these applications are microprocessors or accelerators. Several types of microprocessors based on RSFQ circuits have been demonstrated so far [24, 25, 26].

The hottest topic in the IT category is a reconfigurable data path (RDP) processor [27], which is a compact, high-performance computation engine. The architecture of the RDP processor gives a solution to the memory-wall problem. The memory-wall problem is the problem that the memory bandwidth cannot be wide enough related to the processor performance because of the gap between the operating speed of a processor and that of a memory, and hence, the performance of a computer is limited.

Fig. 7 shows a concept of a computing system based on RSFQ-RDP processors. The RSFQ-RDP processors are used as accelerators, while central processing units (CPUs) based on CMOS devices serve as main processors. An RDP mainly are composed of a 2-dimensional array of floating point number processing units (FPUs). The output of each FPU can be fed to one or more FPUs via flexible operand routing networks (ORNs). Streaming

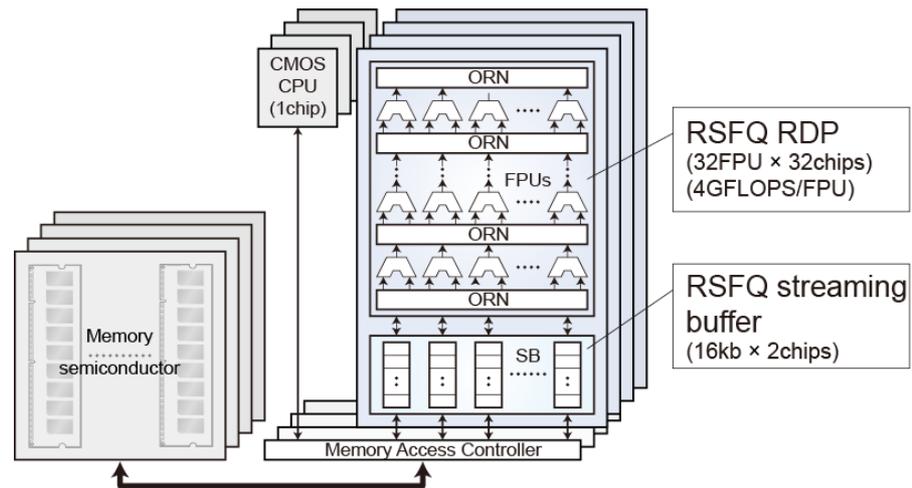


Fig. 7. Concept of a computing system based on the RSFQ RDP processors.

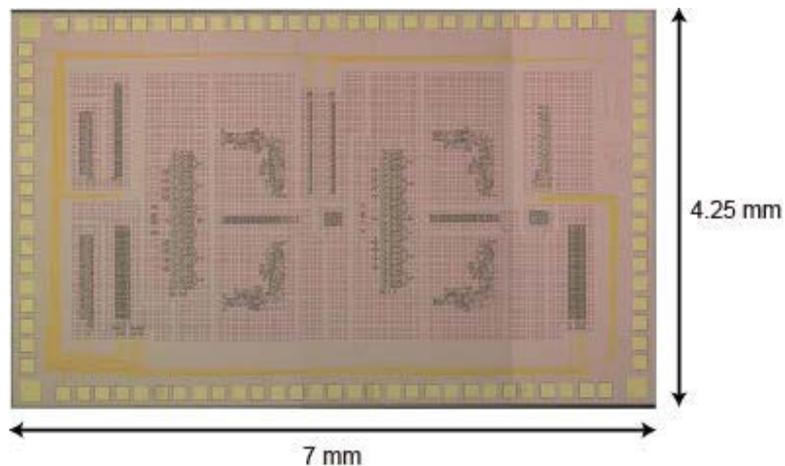


Fig. 8. Microphotograph of a 2×2 RSFQ RDP processor. The processor was designed based on the CONNECT cell library for the ISTEK 10-kA/cm² technology.

buffers are used as temporal buffers for adjustment in the timing between RSFQ RDP processors and CPUs or between RSFQ RDP processors and main memories.

In an RDP, a data flow graph (DFG) extracted from a target application program is mapped to the 2-dimensional FPU array. To enable the mapping, an ORN consists of programmable switches, while FPUs support multiple functions such as add, sub, and multiply. By means of setting the control signals provided to FPUs and ORN switches, the function of the RDP can be changed at run time.

Since the cascaded FPUs can generate a final result without temporally memorizing intermediate data, the number of memory load/store operations corresponding to spill codes is reduced. In other words, memory bandwidth required to achieve high performance can be reduced. Moreover, since a loop-

body mapped into the FPU array is executed in pipeline fashion, RDP can provide high throughput computing.

A microphotograph of a prototype of a 2×2 (double stages of an array composed of dual arithmetic logic units (ALUs)) RDP processor is displayed in Fig. 8. For simplicity, ALUs are employed instead of FPUs in this design. In addition, the ALUs and ORNs are designed to handle only bit-serial data. The RDP processor prototype was made up of 11458 Josephson junctions and occupied an area of $5.61 \times 2.82 \text{ mm}^2$.

All the instructions for each ALU and reconfiguration in the 2×2 RDP processor prototype have been confirmed up to the frequency of 45 GHz. The power consumption is 3.4 mW.

5 New directions in SFQ circuits

In these days, energy efficiency becomes the most important parameter in digital systems. Originally, RSFQ circuits have the special feature of low power/energy consumption. In fact, the intrinsic energy consumption of a Josephson junction within a clock period in RSFQ circuit is roughly expressed as the product of $I_c \Phi_0$, and is estimated to be 0.2 aJ, which is small enough compared to that of semiconductor devices.

Fig. 9 (a) shows an equivalent circuit of a current-driven Josephson junction in RSFQ circuits. As shown in Fig. 1, there are many bias resistors in an actual RSFQ circuits. As a result, Josephson junctions with the bias resistance R_b are considered to be driven by a voltage source of a voltage V_b . The typical value of V_b , R_b , and the shunt resistance R_s are 2.5 mV, 16Ω , and 5Ω , respectively. These values are determined so as to suppress interference between adjacent JJs through bias resistors in high-speed operations. However, much large energy is consumed at a bias resistor, while small energy of $I_c \Phi_0$ is consumed at a shunt resistor.

One of the effective ways to eliminate energy consumption at a bias resistor is employment of ac-biasing. Fig. 9 (b) shows an equivalent circuit of the reciprocal quantum logic (RQL) circuit [7]. As indicated in the figure, ac bias current is supplied to logic gates through a transformer. Adiabatic

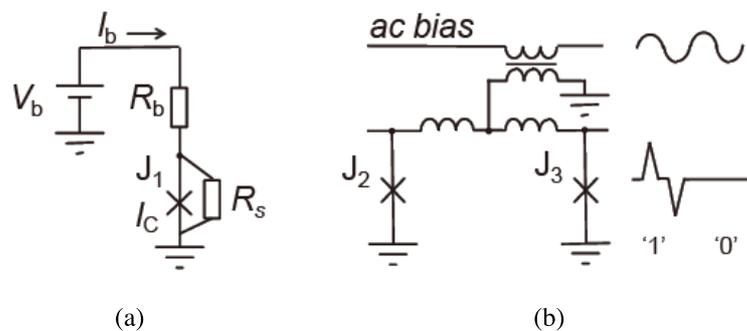


Fig. 9. (a) Equivalent circuit of a current-driven Josephson junction in an actual RSFQ circuit. (b) Equivalent circuit of the RQL. A transformer is used instead of a bias resistor.

quantum flux parametron [9] is also driven by ac bias current. Excellent summary including dc-biased energy-efficient circuits was given at Ref. [8].

Recently, it is found that RSFQ circuits driven with very low voltages such as a few tens or hundreds of μV also exhibit very good energy efficiency. The circuit is named the low-energy RSFQ (LE-RSFQ) circuit [10]. In fact, 20 GHz operation with total energy of about 0.1 aJ consumed at a bias resistor and at a shunt resistor. This energy consumption is close to the Josephson coupling energy $I_c\Phi_0$, although small Josephson junctions with small critical currents are employed.

Experimentally obtained power consumptions and clock periods for LE-RSFQ circuits are plotted in Fig. 2. The PDP values of LE-RSFQ circuits are 1 order of magnitude smaller than those of conventional RSFQ circuits. This small PDP is remarkable advantage to semiconductor devices even if the cooling penalty is taken into account.

6 Conclusion

Operating principle and special features of RSFQ circuits are described. The power-delay products of RSFQ circuits are 4 or 5 orders of magnitude smaller than those of semiconductor devices because of ultra short pulse of a voltage generated across a JJ and release from charging/discharging process for signal transmission. RSFQ-ADC-based and TDC-based digital signal processors have been applied to software-defined radio receivers and superconductor detector array systems, respectively. In these applications, high resolution is achieved by utilizing magnetic flux quantization. RSFQ-ICs are also applied to microprocessors and accelerators. An RSFQ-RDP processor made up of 11000 JJs has been demonstrated up to 45 GHz. Recently, several kinds of energy-efficient SFQ circuits have been proposed and demonstrated. The PDPs of these circuits are 5 or 6 orders of magnitude smaller than those of semiconductor devices. The cooling penalty will be hidden completely and the SFQ-based systems will have distinct advantage to present systems.

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