Improved timing closure by analytical buffer and TSV planning in three-dimensional chips

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Abstract: In this paper, a mathematical solution for integrated buffer and Through-Silicon Via (TSV) planning in three-dimensional chips is presented in which the optimal location of both buffer and TSV of each net is determined simultaneously. In this method, two-dimensional buffer planning formulation is extended to three-dimensional era. Experimental results show that performance and probability of successful buffer/TSV insertion is increased considerably, especially for large and congested three-dimensional circuits.

Keywords: buffer, three-dimensional chip, Through Silicon Via

Classification: Integrated circuits

References


1 Introduction

Three-dimensional or vertical integration is an emerging technology to alleviate the limitations of long interconnects. Many interconnect optimization techniques have been proposed to reduce the delay of global wires such as driver sizing, buffer insertion, wire sizing, and spacing [1]. Buffer insertion is an effective and widely used technique to solve or alleviate the problem [2].
Many contributions have been reported on planning and inserting the buffers in recent years. Buffer block planning was introduced in [3] in which the concept of feasible region (FR) is presented to plan buffers in the dead spaces between blocks in the floorplanning stage of a two-dimensional chip. FR of a buffer is defined as a maximal region in which the buffer may be located such that the delay constraint can be satisfied. In [4], a methodology was presented which considers a percentage of internal macro block area as the buffer site area for inserting buffers. This can improve the quality of buffer insertion in the floorplan stage but several tools and methodologies must be modified to consider the buffer sites inside the macro blocks.

Buffer planning has been widely used in many of research and industrial tools with acceptable results but it cannot be used in three-dimensional chips because in three-dimensional chips, a long wire may travel between tires and therefore two-dimensional feasible regions cannot be used. Moreover, in three-dimensional integrated circuits, a long wire may comprise some through-silicon Vias (TSVs). In this situation, locations of buffers are correlated to the location of TSVs.

Authors of [2], proposed a simulated annealing-based buffer and interlayer via planning algorithm with linear complexity. Authors of [2] divided the simulated annealing process into three phases to speed up the algorithm: area optimization, timing optimization and buffer and interlayer Via planning. In [5], a buffer planning algorithm is proposed at floorplanning stage for three-dimensional ICs in which at first buffer insertion is reduced to a dynamic programming path problem. At the same time, vertical interlayer Vias is also planned. At last, buffer planning is integrated with floorplanning to optimize the packing so that not only area and wire length reach a satisfying value, timing performance is also optimized.

In this paper, we proposed an analytical solution for optimal integrated buffer and TSV planning to find out the best location of both buffers and TSVs of each net. In this work, the concept of feasible region is extended to feasible surfaces in third dimension. Our analysis shows that the number of possible locations for buffers and TSVs can be extremely larger on feasible surface rather than two-dimensional buffer regions. Therefore, these resources can be inserted more freely to meet the timing closure of design.

This paper is organized as follows. Section 2, describes buffer planning techniques for two-dimensional chips and the proposed three-dimensional planning solution is presented in Section 3. Experimental results and analyses are represented in Section 4 and finally, Section 5 concludes the paper.

2 Two-dimensional buffer block planning

As mentioned before, this paper is mainly focused on extending the two-dimensional buffer block planning to three-dimensional domain. Therefore, we reviewed the concept of two-dimensional buffer planning in this section to simplify describing the proposed method. Cong et al. in [3] presented a mathematical formulation for planning the location of buffers before or
during the placement.

Cong’s formulation was based on the feasible region (FR) concept. For a single buffer that is inserted on a long wire at distance $x$ from the driver, the Elmore delay from the driver to the sink is [3]:

$$T = r.c.x^2 - [(R_b - R_d).c + r.(C_L - C_b) + r.c.l].x + R_d.C_b + T_b + R_b.(C_L + c.l) + \frac{1}{2}r.c.l^2 + r.l.C_L$$

where, $l$ is the wire length ($\mu$m), $r$ is the unit length wire resistance ($\Omega/\mu$m), $c$ is the unit length wire capacitance ($fF/\mu$m), $T_b$ is the intrinsic delay of buffer ($ps$), $C_b$ is the input capacitance of the buffer ($fF$), $R_d$ and $R_b$ are the output resistances of driver and the buffer ($\Omega$), respectively and $C_L$ is the load capacitance at output of the wire ($fF$). In the canonical design flow, a required delay ($T_{req}$) for each net of the design is calculated based on the input delay constraints (Eq. (2)).

$$T_{req} = r.c.x^2 - [(R_b - R_d).c + r.(C_L - C_b) + r.c.l].x + R_d.C_b + T_b + R_b.(C_L + c.l) + \frac{1}{2}r.c.l^2 + r.l.C_L$$

The feasible region of each buffer showing the possible start and end point of the buffer such that the delay is less than ($T_{req}$), can be calculated by solving the quadratic Eq. (2) with respect to $x$. Range of the feasible region $[x_{min}, x_{max}]$ is as:

$$[x_{min}, x_{max}] = \left[ max \left(0, \frac{K_2 - \sqrt{K_2^2 - 4K_1K_3}}{2K_1}\right), \min \left(l, \frac{K_2 + \sqrt{K_2^2 - 4K_1K_3}}{2K_1}\right)\right]$$

where

$$K_1 = r.c, \quad K_2 = (R_b - R_d).c + (C_L - C_b).r + r.c.l \quad K_3 = R_d.C_b + T_b + R_b.(C_L + c.l) + \frac{1}{2}r.c.l^2 + r.l.C_L - T_{req}$$

3 Proposed three-dimensional buffer block planning

In regular design flow, buffers can be planned during the placement or after it. Main drawback of the first approach is that locations of cells are not fixed and consequently, buffers may plan at inappropriate location. However, location of the cells and global topology of the nets are determined after the placement and locations of the buffers can be estimated correctly but it is possible that no white space be found to place the buffer because location of other cells has been fixed. Second approach (i.e. buffer/TSV insertion after placement) is more popular in real EDA tools. Therefore, we try to improve the second approach.

In a three-dimensional chip, cells are distributed on various tiers (e.g. planes) and wires may span between the tiers. Therefore, inserting a buffer along a net depends on the location of the TSV that connects terminals
of a net on a plane to the terminals on other planes. Figure 1 (a) shows an example of three-dimensional buffer and TSV planning. As shown in Figure 1 (a), buffer can be inserted before or after the TSV. It is noting that location of TSV and buffer of a net are not independent parameters and affect on each other. Three-dimensional connection (Figure 1 (a)) can be modeled as a two-dimensional connection as shown in Figure 1 (b).

Figure 2 shows the proposed RC model of two-dimensional wire comprising of a buffer and a TSV. In this figure, \( l, x \) and \( y \) show the length of the wire, buffer distance from the driver and TSV distance from the buffer, respectively. In this paper, we assumed that buffer should be inserted before the TSV. However, the proposed formulation can be changed easily for the situation that buffer be inserted after the TSV. In the presented model (as shown in Figure 2), buffer and TSV are inserted at the appropriate distance to minimize the delay of the buffered wire. It is worth note that Figure 2 is RC model of Figure 1 (b).

In Figure 2, \( R_{TSV} \) and \( C_{TSV} \) are the resistance and capacitance of TSV, respectively and other parameters are the same as the parameters described in Section 2. Delay of the wire shown in Figure 2 can be calculated as:

\[
T = R_d (c.x + C_b) + r.x \left( \frac{1}{2} c.x + C_b \right) + T_b
+ R_b [c.y + C_{TSV} + c(l - y - x) + C_L]
+ r.y \left[ \frac{1}{2} c.y + C_{TSV} + \frac{1}{2} c.(l - y - x) + C_L \right]
+ R_{TSV} [C_{TSV} + c.(l - y - x) + C_L]
+ r(l - y - x) \left[ \frac{1}{2} c.(l - y - x) + C_L \right]
\]

where \( r \) and \( c \) are the intrinsic unit length resistance and capacitance of the wire, respectively. We used the parameters presented in [3] for our calculations throughout the paper. By substituting these parameters into Eq. (5), the
following equation is obtained:

$$T_{opt} = A.x^2 + B.y^2 + C.x + D.y + E.x.y + F$$  \( (6) \)

As mentioned before, the main objective of buffer and TSV planning is to find the best position for buffer and TSV on a wire such that the wire delay is minimized. Therefore, we differentiate the Eq. (6) with respect to \( x \) and \( y \) to compute \( T_{opt} \). Then, two equations with two variables is obtained that can be solved in order to achieve the optimal values for \( x \) and \( y \). By substituting the optimal values of \( x \) and \( y \) in Eq. (6), optimum delay (\( T_{opt} \)) is calculated. In real design process, \( T_{req} \) is determined by designers as a major design constraint. It is clear that the value of \( T_{req} \) is larger than \( T_{opt} \). It can be easily shown that there is no real root for Eq. (7) when the value of \( T_{req} \) is smaller than \( T_{opt} \). When the value of \( T_{req} \) is larger than \( T_{opt} \), two roots are obtained for \( x \) and \( y \), which is \((x_{min}, x_{max})\) and \((y_{min}, y_{max})\), respectively. All the values between these two roots are the feasible locations. It is worthwhile to note that feasible region represents an ellipse and enormous number of feasible points can be chosen on this ellipse for buffer and TSV. Eq. (7) to Eq. (10) can be used to obtain \((x_{min}, x_{max})\):

$$A.x^2 + B.y^2 + C.x + D.y + E.x.y + G = T_{req}$$  \( (7) \)

Assuming that \( G = F - T_{req} \), we have:

$$A.x^2 + B.y^2 + C.x + D.y + E.x.y + G = 0$$  \( (8) \)

By differentiating the Eq. (8) with respect to \( y \), we have:

$$2B.y + D + E.x = 0 \Rightarrow y = \frac{-E.x - D}{2B}$$  \( (9) \)

By Substituting the Eq. (9) in Eq. (8), the Eq. (10) is obtained as:

$$\left( A - \frac{E^2}{4B}\right).x^2 + \left( C - \frac{DE}{2B}\right).x + \left( G - \frac{D^2}{4B}\right) = 0$$  \( (10) \)

where the value of \((x_{min}, x_{max})\) can be computed by solving Eq. (10) and this process can be repeated for calculating \((y_{min}, y_{max})\).

It is worth noting that each buffer should be inserted inside its feasible region if required white space is found in the feasible region. In a wide feasible region, the probability of finding a suitable white space will be increased. As mentioned before, feasible region for the buffer and TSV has enormous possible values. After finding the feasible region, a feasible location is selected for buffer and TSV inside or near the white spaces of the design. TSV/buffer insertion is successful when a free location can be found for it on feasible responses of Eq. (10) otherwise TSV/buffer insertion will be failed.

4 Experimental results

We have implemented our buffer/TSV planning algorithms using C++ on an Intel dual core machine with 2 GB of main memory. The parameters used in
our experiments are based on [3]. We have tested our algorithms on 9 benchmarks of IWLS benchmark suite. All the benchmarks are partitioned using hMetis into 3 partitions (tiers) and place each tier using DragonPlacer [6] for three-dimensional placement.

Table I shows comparison of the results of proposed planning with the one presented in [5]. In this Table I, columns #Cell, #LW and #Buf show the number of cells, number of long wires and number of buffers planned in the circuits, respectively. Column Fail represents the percent of TSV/buffer insertion that fails and column and DI shows the percentage of Elmore delay improvement after buffer/TSV insertion. Finally, column Total DI shows the delay improvement of the proposed planning compared with the approach of [5].

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>#Cell</th>
<th>#LW</th>
<th>Proposed Planning #Buf</th>
<th>Fail (%)</th>
<th>DI (%)</th>
<th>Approach of [5] #Buf</th>
<th>Fail (%)</th>
<th>DI (%)</th>
<th>Total DI (%)</th>
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<tr>
<td>b17</td>
<td>37117</td>
<td>11</td>
<td>0.0</td>
<td>6.05</td>
<td>0</td>
<td>100.0</td>
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<td>22</td>
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<td>ethernet</td>
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<td>129</td>
<td>129</td>
<td>0.0</td>
<td>10.14</td>
<td>480</td>
<td>8.60</td>
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<tr>
<td>b19</td>
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<td>436</td>
<td>0.0</td>
<td>10.14</td>
<td>480</td>
<td>8.60</td>
<td>17.91</td>
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<tr>
<td>b20</td>
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<td>128</td>
<td>9.94</td>
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<td></td>
<td></td>
<td></td>
<td></td>
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</table>

As can be seen in Table I, the proposed buffer insertion is more suitable for large circuits because the large circuits have more number of long wires and thus have more potential for buffer insertion. Moreover, the percentage of successful buffer insertion is considerably more than [5] because feasible region of the proposed planning method is wider.

5 Conclusion

In this paper, a simultaneous buffer and TSV planning method is proposed for three-dimensional chips that simplifies finding optimal location for buffer and TSV concurrently such that delay constraints are satisfied. Experimental results show that the presented planning leads to significant improvement over previous methods in terms of delay and buffer/TSV insertion success rate.